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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-SY*-A030A/E	Rev.	1.00
Title	Additional updates for current version of the User's Manual		Information Category	Technical Notification		
Applicable Product	Renesas Synergy™ S7G2, S5D9, S5D5, S3A7, S3A6, S3A3, S128, and S124 MCU Groups	Lot No. All lots	Reference Document	See below.		

This Technical Update describes corrections for published User's Manuals of Synergy Microcontrollers. You can search for the affected User's Manual by its document number shown in parenthesis ( ).
S7G2 Rev.1.20 (R01UM0001EU0120), S5D9 Rev.1.00 (R01UM0004EU0100),
S5D5 Rev.1.10 (R01UM0009EU0110), S3A7 Rev.1.20 (R01UM0002EU0120),
S3A6 Rev.1.00 (R01UM0007EU0100), S3A3 Rev.1.00 (R01UM0006EU0100),
S124 Rev.1.20 (R01UM0003EU0120), and S128 Rev.1.00 (R01UM0005EU0100)

[Changes summary]

Chapter	Item	Description	S7G2	S5D9	S5D5	S3A7	S3A6	S3A3	S124	S128
GPT	1, 2, 3, 4, 5	Removed description of rotation direction control	✓	✓	✓	✓	✓	✓	✓	✓
USBFS	6, 7	Removed description of connected through the hub	-	-	-	✓	✓	✓	-	-

Note:
The locations where corrections are made in the User's Manual can be in a paragraph, table, figure, sub-section, and section in a chapter. Depending on the product manuals that are affected, the chapter number can be different. For example, the GPT chapter of the S7G2 MCU User's Manual is chapter 23 but for the S124 MCU User's Manual, this is chapter 19. In the User's Manual, a section, table, or figure number is preceded by the chapter number. When a chapter, section, sub-section, table, or figure number is different, n and m are used to express them as explained in the following pages.

1. (All Series) General PWM Timer (GPT), n.2.m Output Phase Switching Control Register (OPSCR)

[Before]

n.2.XX Output Phase Switching Control Register (OPSCR)

Address(es): GPT_OPS.OPSCR 4007 8FF0h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	NFCS[1:0]		NFEN	—	—	GODF	GRP[1:0]		—	—	ALIGN	RV	INV	N	P	FB
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	EN	—	W	V	U	—	WF	VF	UF
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b20	RV	Output Phase Rotation Direction Reversal	0: Output U/V/W-phase 1: Output reverse of V/W-phase	R/W

[After]

n.2.XX Output Phase Switching Control Register (OPSCR)

Address(es): GPT_OPS.OPSCR 4007 8FF0h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	NFCS[1:0]		NFEN	—	—	GODF	GRP[1:0]		—	—	ALIGN	—	INV	N	P	FB
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	EN	—	W	V	U	—	WF	VF	UF
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b20	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

2. (All Series) General PWM Timer (GPT), n.3.11 Output Phase Switching (GPT_OPS)

[Before]

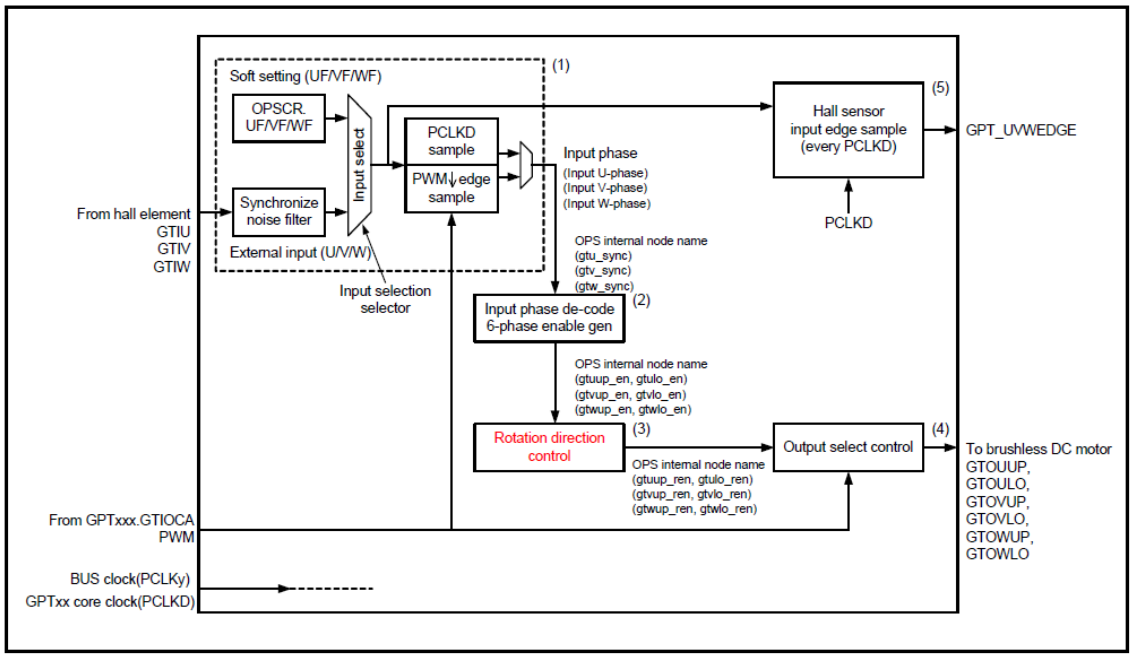

Figure n.m Conceptual diagram of GPT OPS control flow

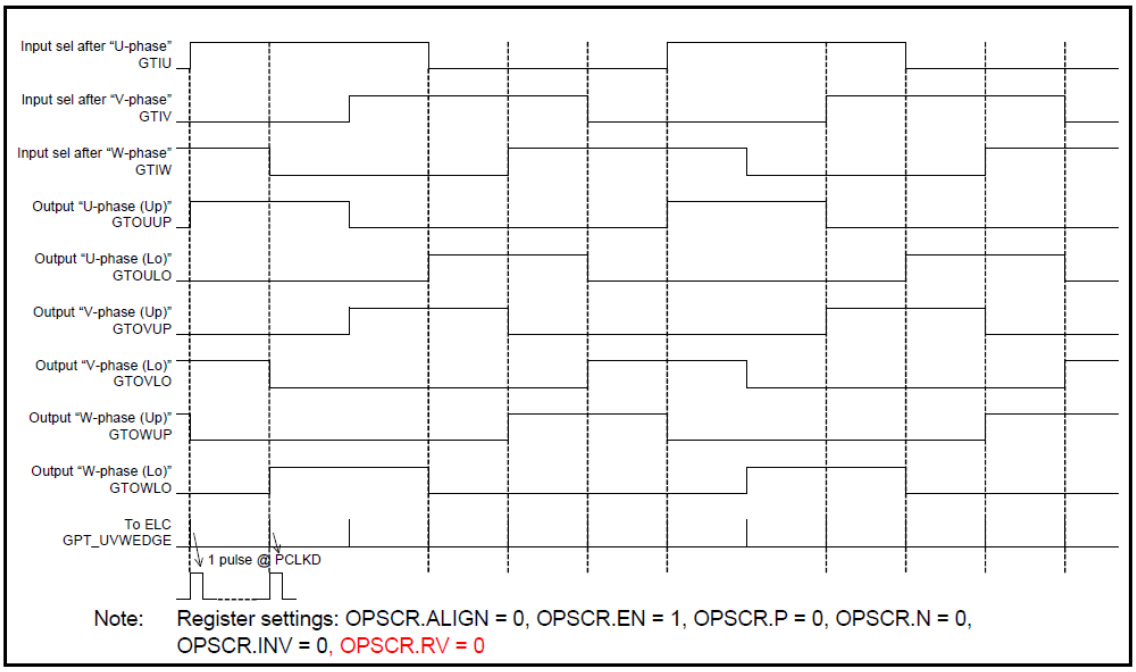

Figure n.m+1 Example of 6-phase level output operation

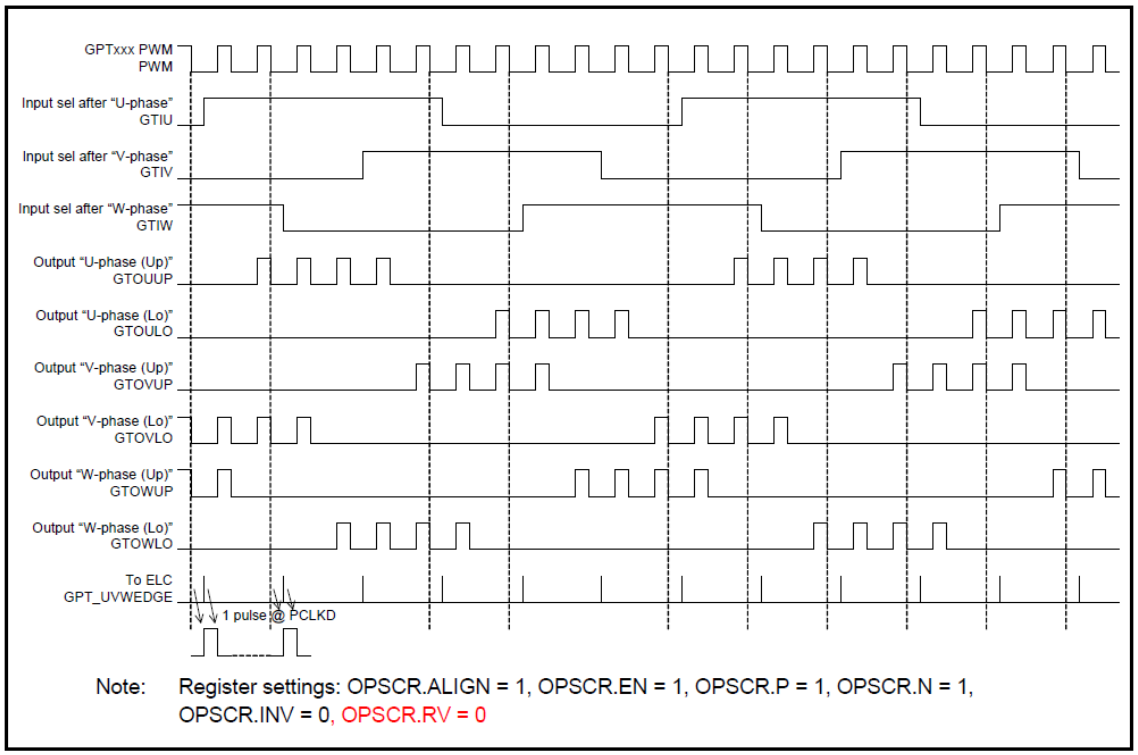

Figure n.m+2 Example of 6-phase PWM output operation with chopper control

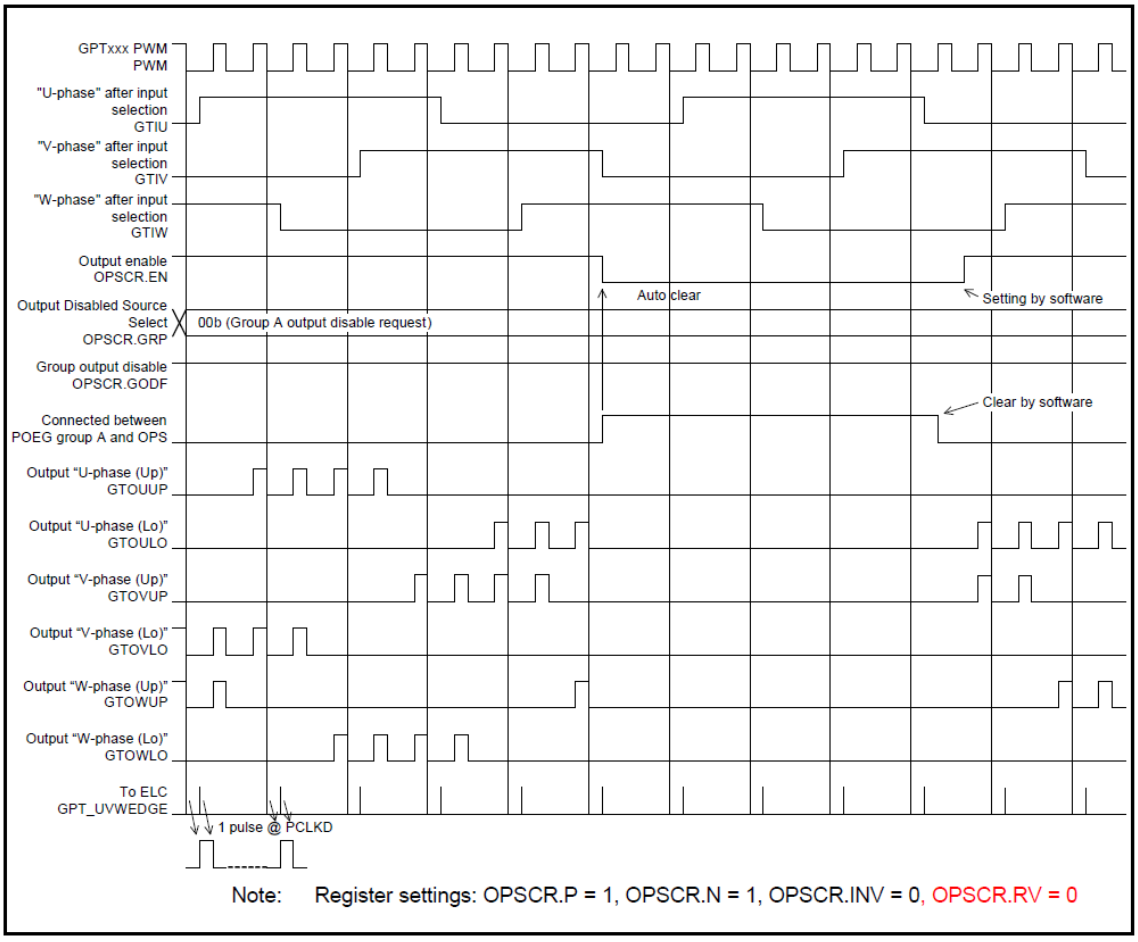

Figure n.m+3 Example of group output disable control operation

[After]

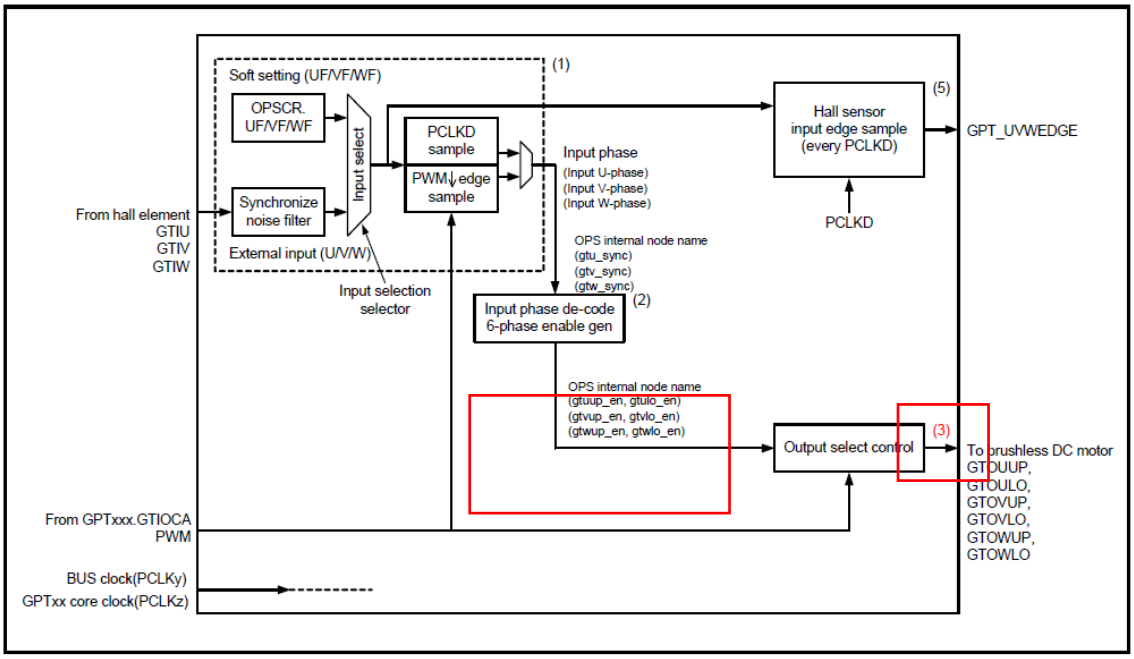

Figure n.m Conceptual diagram of GPT_OPS control flow

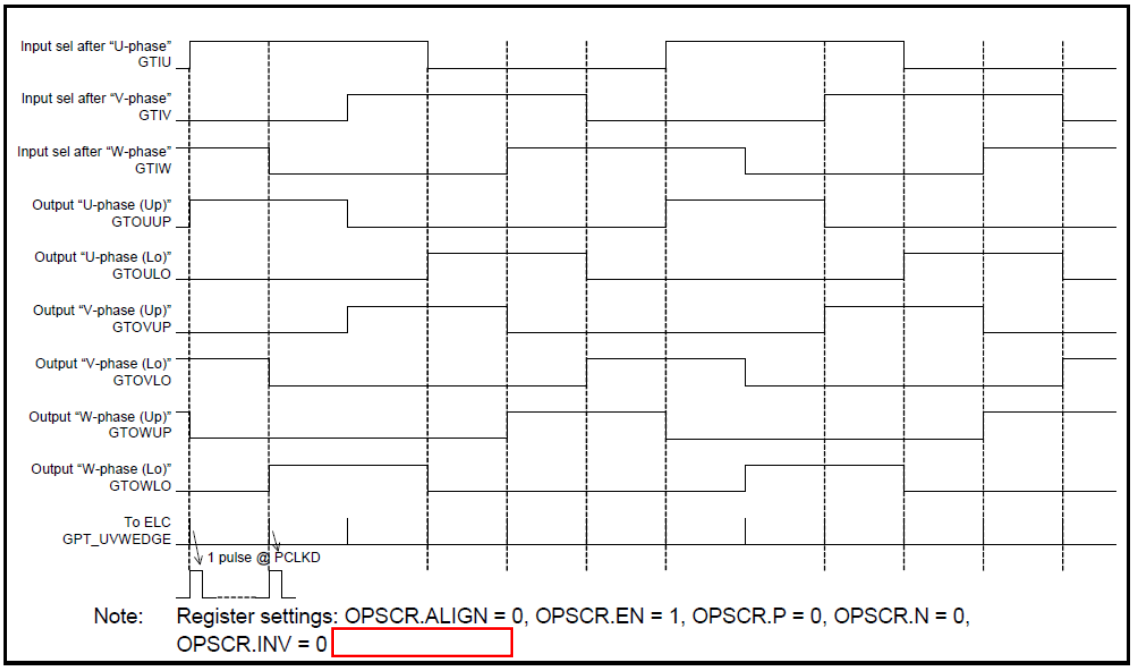

Figure n.m+1 Example of 6-phase level output operation

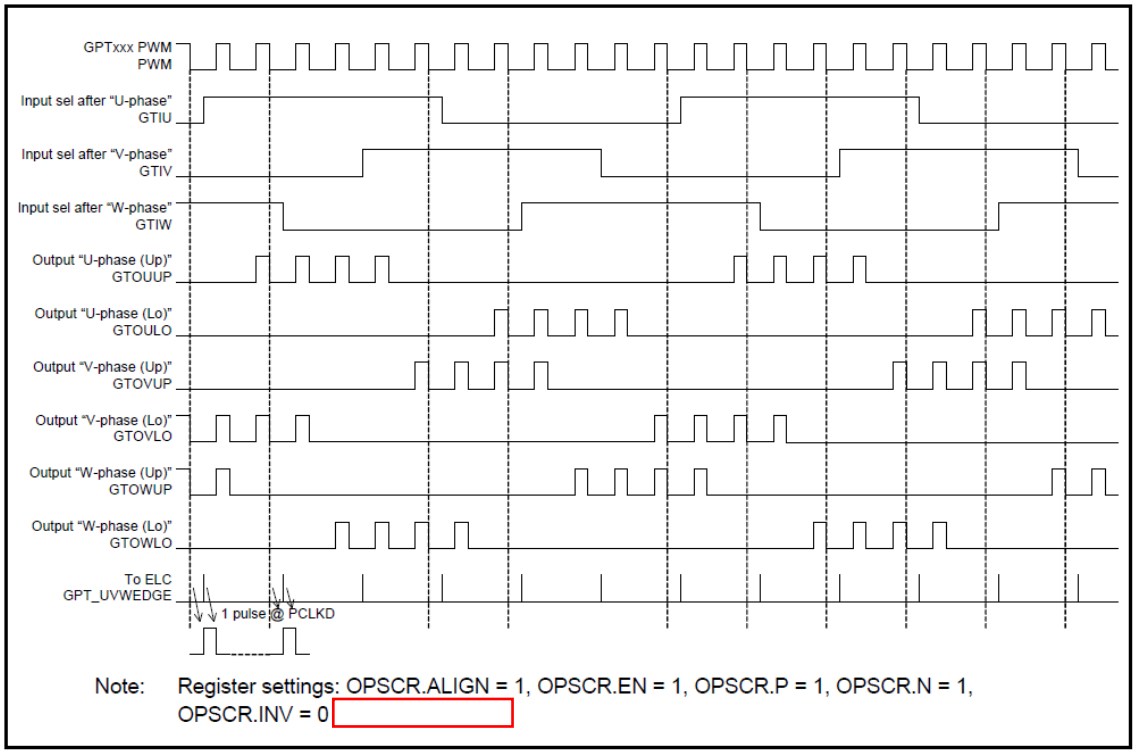

Figure n.m+2 Example of 6-phase PWM output operation with chopper control

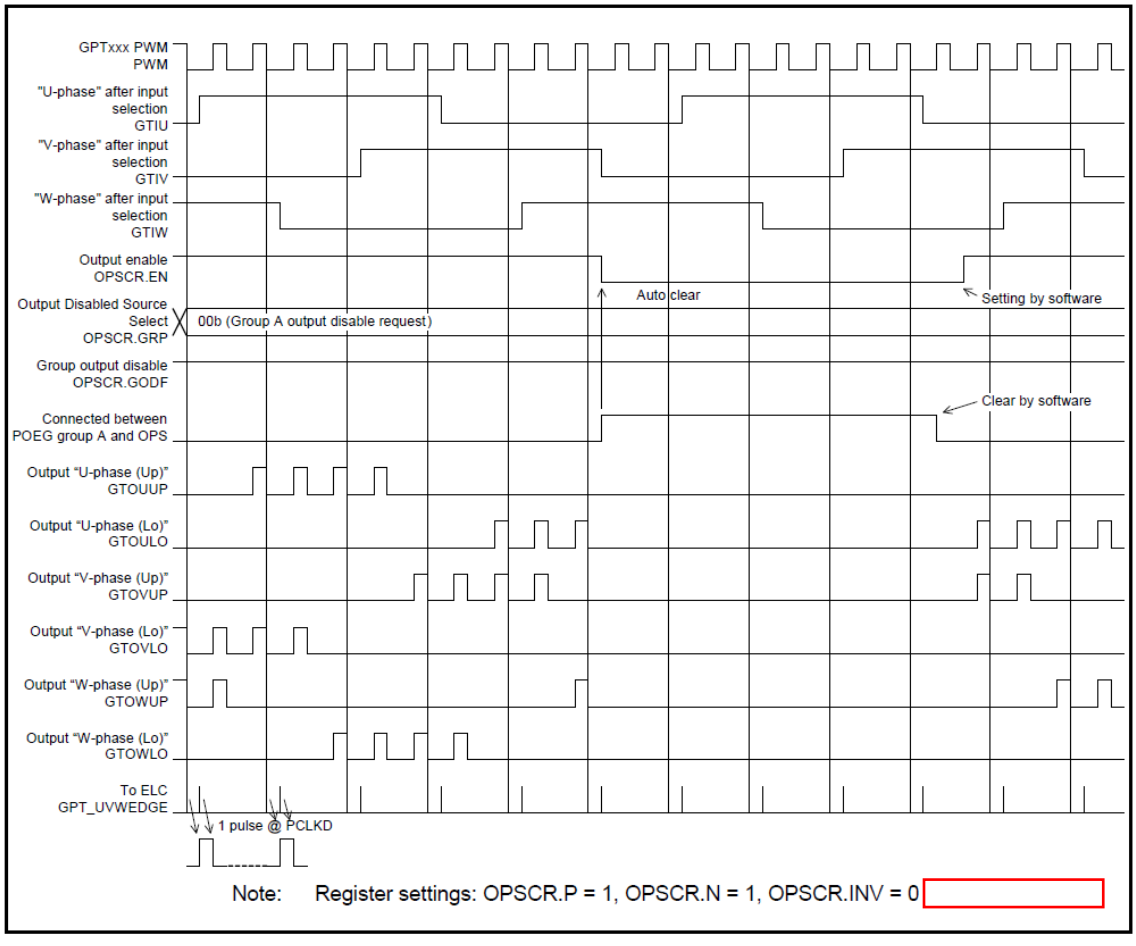

Figure n.m+3 Example of group output disable control operation

3. (All Series) General PWM Timer (GPT), n.3.11.4 Rotation direction control

[Before]

In the GPT_OPS control flow conceptual diagram shown in Figure 23.81, (3) controls the direction of rotation of a 3-phase motor using the OPSCR.RV bit. When OPSCR.RV bit = 1, it reverses the direction of rotation of the OPSCR.RV bit = 0 setting by replacing the V-phase and W-phase.

Table 23.20 shows the allocation of the output phase to the OPSCR.RV bit (rotation direction control execution before and after).

Table n.m Rotation direction control method

OPSCR register output phase rotation direction reversal	**Output of rotation direction control [U/V/W (pos/neg)]**					
	(OPS internal node name of the control after)					
OPSCR.RV bit	**(gtuup_ren)**	**(gtulo_ren)**	**(gtvup_ren)**	**(gtvlo_ren)**	**(gtwup_ren)**	**(gtwlo_ren)**
0	U-phase (up) (gtuup_en)	U-phase (low) (gtulo_en)	V-phase (up) (gtvup_en)	V-phase (low) (gtvlo_en)	W-phase (up) (gtwup_en)	W-phase (low) (gtwlo_en)
1	U-phase (up) (gtuup_en)	U-phase (low) (gtulo_en)	W-phase (up) (gtwup_en)	W-phase (low) (gtwlo_en)	V-phase (up) (gtvup_en)	V-phase (low) (gtvlo_en)

[After]

Removed.

4. (All Series) General PWM Timer (GPT), n.3.11.5 Output selection control

[Before]

In the GPT_OPS control flow conceptual diagram in Figure XX.YY, (4) presents the selection of the output waveform by setting the OPSCR register bit.

Table n.m Output selection control method (positive phase)

Enable-phase output control	Positive-phase output (P) control	Invert-phase output control	Output port name (positive phase = up) (output selection internal node allocation)	
OPSCR.EN bit	OPSCR.P bit	OPSCR.INV bit	GTOUUP GTOVUP GTOWUP	Mode
0	x	x	0	Output Stop (External pin Hi-Z) GPT_OPS=> 0 output
1	0	0	Level signal (gtuup_ren) (gtvup_ren) (gtwup_ren)	Level Output mode (Positive phase) (Positive logic)
1	0	1	Level signal (~gtuup_ren) (~gtvup_ren) (~gtwup_ren)	Level Output mode (Positive phase) (Negative logic)
1	1	0	PWM signal (PWM & gtuup_ren) (PWM & gtvup_ren) (PWM & gtwup_ren)	PWM Output mode (Positive phase) (Positive logic)
1	1	1	PWM signal (~(PWM & gtuup_ren)) (~(PWM & gtvup_ren)) (~(PWM & gtwup_ren))	PWM Output mode (Positive phase) (Negative logic)

Table n.m+1 Output selection control method (negative phase)

Enable-phase output control	Positive-phase output (N) control	Invert-phase output control	Output port name (negative phase = low) (output selection internal node allocation)	
OPSCR.EN bit	OPSCR.N bit	OPSCR.INV bit	GTOUUP GTOVUP GTOWUP	Mode
0	x	x	0	Output Stop (External pin Hi-Z) GPT_OPS=> 0 output
1	0	0	Level signal (gtulo_ren) (gtvlo_ren) (gtwlo_ren)	Level Output mode (Negative phase) (Positive logic)
1	0	1	Level signal (~gtulo_ren) (~gtvlo_ren) (~gtwlo_ren)	Level Output mode (Negative phase) (Negative logic)
1	1	0	PWM signal (PWM & gtulo_ren) (PWM & gtvlo_ren) (PWM & gtwlo_ren)	PWM Output mode (Negative phase) (Positive logic)
1	1	1	PWM signal (~(PWM & gtulo_ren)) (~(PWM & gtvlo_ren)) (~(PWM & gtwlo_ren))	PWM Output mode (Negative phase) (Negative logic)

[After]

In the GPT_OPS control flow conceptual diagram in Figure XX.YY, (3) presents the selection of the output waveform by setting the OPSCR register bit.

Table n.m Output selection control method (positive phase)

Enable-phase output control	Positive-phase output (P) control	Invert-phase output control	Output port name (positive phase = up) (output selection internal node allocation)	
OPSCR.EN bit	OPSCR.P bit	OPSCR.INV bit	GTOUUP GTOVUP GTOWUP	Mode
0	x	x	0	Output Stop (External pin Hi-Z) GPT_OPS=> 0 output
1	0	0	Level signal (gtuup_en) (gtvup_en) (gtwup_en)	Level Output mode (Positive phase) (Positive logic)
1	0	1	Level signal (~gtuup_en) (~gtvup_en) (~gtwup_en)	Level Output mode (Positive phase) (Negative logic)
1	1	0	PWM signal (PWM & gtuup_en) (PWM & gtvup_en) (PWM & gtwup_en)	PWM Output mode (Positive phase) (Positive logic)
1	1	1	PWM signal (~(PWM & gtuup_en)) (~(PWM & gtvup_en)) (~(PWM & gtwup_en))	PWM Output mode (Positive phase) (Negative logic)

Table n.m+1 Output selection control method (negative phase)

Enable-phase output control	Negative-phase output (N) control	Invert-phase output control	Output port name (negative phase = low) (output selection internal node allocation)	
OPSCR.EN bit	OPSCR.N bit	OPSCR.INV bit	GTOUUP GTOVUP GTOWUP	Mode
0	x	x	0	Output Stop (External pin Hi-Z) GPT_OPS=> 0 output
1	0	0	Level signal (gtulo_en) (gtvlo_en) (gtwlo_en)	Level Output mode (Negative phase) (Positive logic)
1	0	1	Level signal (~gtulo_en) (~gtvlo_en) (~gtwlo_en)	Level Output mode (Negative phase) (Negative logic)
1	1	0	PWM signal (PWM & gtulo_en) (PWM & gtvlo_en) (PWM & gtwlo_en)	PWM Output mode (Negative phase) (Positive logic)
1	1	1	PWM signal (~(PWM & gtulo_en)) (~(PWM & gtvlo_en)) (~(PWM & gtwlo_en))	PWM Output mode (Negative phase) (Negative logic)

5. (All Series) General PWM Timer (GPT), n.3.11.8 GPT_OPS start operation setting flow

[Before]

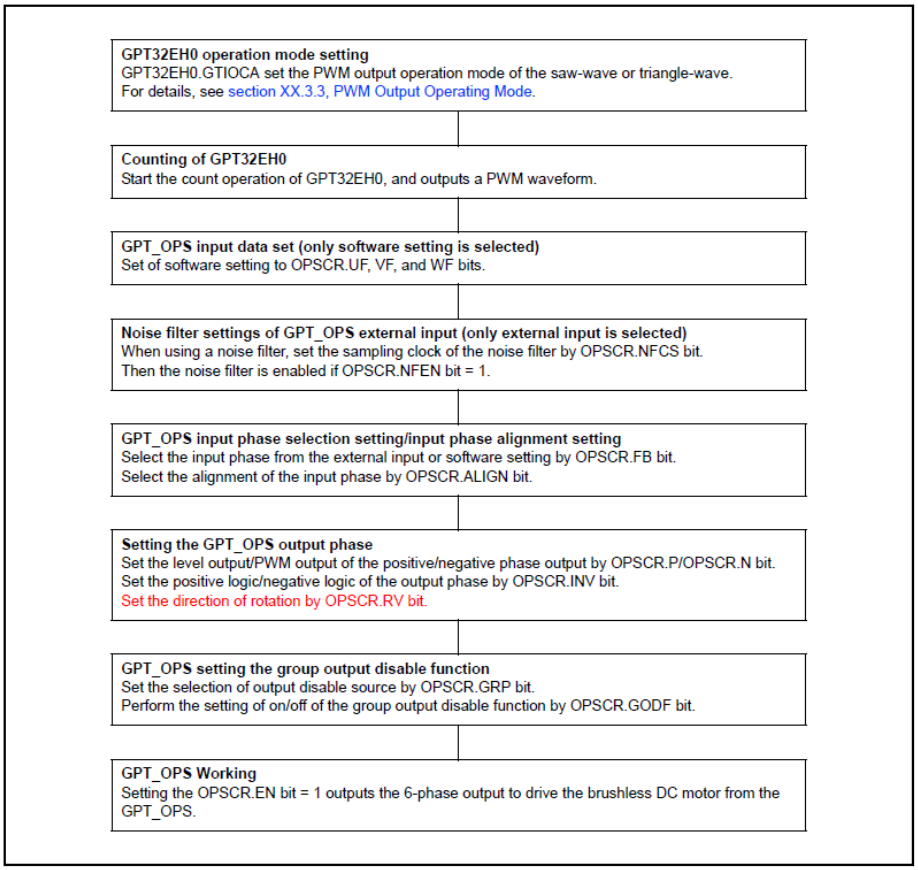

Figure XX.YY Example setting for of GPT_OPS start operation

[After]

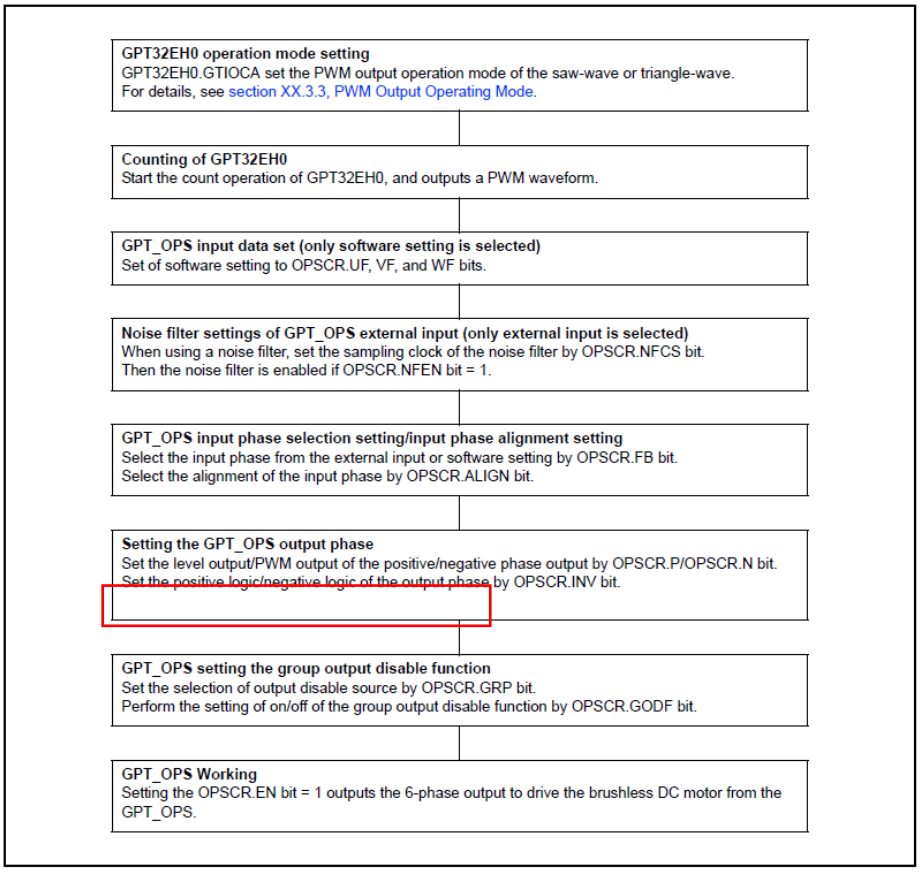

Figure XX.YY Example setting for of GPT_OPS start operation

6. (S3 Series) USB 2.0 Full-Speed Module (USBFS), Table n.1 USBFS specifications

[Before]

Item	Specifications
Features	Host controller features: ● Full-speed transfer (12 Mbps) and low-speed transfer (1.5 Mbps) ● Automatic scheduling for SOF and packet transmissions ● Programmable intervals for isochronous and interrupt transfers ● Communications with multiple peripheral devices connected through a single hub.

[After]

Item	Specifications
Features	Host controller features: ● Full-speed transfer (12 Mbps) and low-speed transfer (1.5 Mbps) ● Automatic scheduling for SOF and packet transmissions ● Programmable intervals for isochronous and interrupt transfers ~~● Communications with multiple peripheral devices connected through a single hub.~~

7. (S3 Series) USB 2.0 Full-Speed Module (USBFS), n.2.33 Device Address n Configuration Register (DEVADDn) (n = 0 to 5)

[Before]

USBSPD[1:0] bits (Transfer Speed of Communication Target Device)

The USBSPD[1:0] bits specify the USB transfer speed of the target peripheral device.

Set these bits to 10b when a full-speed device is connected through the hub. In host controller mode, the USBFS generates packets based on the USBSPD[1:0] setting. In device controller mode, set these bits to 00b.

[After]

USBSPD[1:0] bits (Transfer Speed of Communication Target Device)

The USBSPD[1:0] bits specify the USB transfer speed of the target peripheral device.

~~Set these bits to 10b when a full-speed device is connected through the hub.~~ In host controller mode, the USBFS generates packets based on the USBSPD[1:0] setting. In device controller mode, set these bits to 00b.