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Old Company Name in Catalogs and Other Documents

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GRADE A

MSC TECHNICAL NEWS

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7700 Series Remarks on Interrupts

In certain cases, caution is required when **writing** to the 7700 Series interrupt control registers.

1. Relevant types
   This applies to the following groups, regardless of the memory type, memory capacity, speed, or operating voltage etc.

   M37700, M37701, M37702, M37703, M37704, M37705, M37708, M37720, M37730, M37732

2. The problem
   The problem occurs when special programs are executed, that use instructions such as LDM to write all bits to the interrupt control register of interrupts for which the interrupt request is asynchronously generated. Accordingly, there is no problem at all when these interrupt control registers are being accessed by the normal programming method using the CLB and SEB instructions.

   2.1 The present condition
   If the interrupt control registers for two interrupt sources are at an even address and the following (even address+1) odd address, and a **write instruction W** (refer to 2.3 for details) is being used to write to one of the registers only, if an interrupt request occurrs for the other register, the interrupt request bit for the latter is not set to "1".

   The case in which the instruction is one that changes the data length using the data length flag (m) is described below. The case in which the instruction is one that changes the data length using the index register length flag (x) is the same.

   For example, when the data length flag (m) is "1" (8-bit), and an interrupt control register at an even address is being written to, there is a possibility that the interrupt request bit of the following odd address will be effected, and when an interrupt control register at an odd address is being written to, there is a possibility that the interrupt request bit of the previous even address will be effected.

   Also, when the data length flag (m) is "0" (16-bit), and a write is performed from an interrupt control register at an odd address, the write operation is actually performed in two cycles. Therefore, in the same way as for the case when the data length flag (m) is "1", there is a possibility that the interrupt request bit of the previous even address will be effected when an interrupt control register at an odd address is being written to, and when an interrupt control register at an even address is being written to, there is a possibility that the interrupt request bit of the following odd address will be effected.

Mitsubishi has upgraded the 7700/7701/7720 Groups as shown below. All functions of each original group have been included in the newer models. Please use the upgraded models as indicated:

Original Model	Upgraded Model
7700 Group	7702 Group
7701 Group	7703 Group
7720 Group	7721 Group

In addition, please note that Mitsubishi is no longer accepting orders for the 7730 Group.
For other alternatives, please take a look at the 7702/7732/7733 Groups.

When the data length flag (m) is "0" (16-bit), and a write instruction is executed from an even address, the write operation is performed in one cycle and neither of the interrupt request bits are effected.

2.2 Relevant registers

The relationship between the registers that produce an effect because of the write operation described above, and the registers that are effected and have their interrupt request bits cleared to "0", is given in the table below.

Note, however, with the $\overline{INT_0}$ and $\overline{INT_1}$ interrupt requests, as there is no influence from write operations to the timer B2 and $\overline{INT_2}$ interrupt control registers, the interrupt request bit is not cleared to "0". Also, watchdog timer interrupt and $\overline{DBC}$ interrupt, which do not have interrupt control registers, are not effected.

Interrupt control registers that produce an effect because of the write operation.		Interrupt control registers that have their interrupt request bits cleared to "0".		Remarks
Interrupt source	address	Interrupt source	address	
DMA0	$6C_{16}$	DMA1	$6D_{16}$	Only applies to M37720
DMA1	$6D_{16}$	DMA0	$6C_{16}$	
DMA2	$6E_{16}$	DMA3	$6F_{16}$	
DMA3	$6F_{16}$	DMA2	$6E_{16}$	
A-D conversion	70_{16}	UART0 transmission	71_{16}	
UART0 transmission	71_{16}	A-D conversion	70_{16}	Except M37730
UART0 receive	72_{16}	UART1 transmission	73_{16}	Except M37730
UART1 transmission	73_{16}	UART0 receive	72_{16}	
UART1 receive	74_{16}	Timer A0	75_{16}	
Timer A0	75_{16}	UART1 receive	74_{16}	Except M37730
Timer A1	76_{16}	Timer A2	77_{16}	
Timer A2	77_{16}	Timer A1	76_{16}	
Timer A3	78_{16}	Timer A4	79_{16}	
Timer A4	79_{16}	Timer A3	78_{16}	
Timer B0	$7A_{16}$	Timer B1	$7B_{16}$	Except M37730
Timer B1	$7B_{16}$	Timer B0	$7A_{16}$	
$\overline{INT_0}$	$7D_{16}$	Timer B2	$7C_{16}$	Except M37730
$\overline{INT_1}$	$7E_{16}$	$\overline{INT_2}$	$7F_{16}$	Except M37705

2.3 Relevant instructions

Write instructions covered by the "write instruction W" described in 2.1 above are as follows.

LDM, STA, STX, STY

In general the CLB and SEB instructions are used to write to this area, and use of these instructions will not cause any problems.

Also, although they are probably not normally executed in this area, the problem that occurs when the LDM instruction is used also occurs with the following instructions.

BRK, JSR, MVN, MVP, PEA, PEI, PER, PHA, PHB, PHD, PHG, PHP, PHT, PHX, PHY, PSH

3. Countermeasures

When writing to an interrupt control register with the data length flag (m) (or the index register length flag (x)) set to "1" (8-bit), or when word writing from an odd address with the data length flag (m) (or the index register length flag (x)) set to "0" (16-bit), **use the CLB and SEB instructions** to set the necessary bits in the interrupt control register.

Program example (with the data length flag (m) set to "1" (8-bit))

• To disable interrupts (set the interrupt priority level to "0")

```
CLB.B     #07H, XXXX
```

• To set the interrupt priority level to "3"

```
CLB.B     #07H, XXXX
SEB.B     #03H, XXXX
```

As touched upon in 2.1 above, when the data length flag (m) (or the index register length flag (x)) is "0" (16-bit), and a word writing is executed from an even address, the write operation is performed in one cycle, and neither of the interrupt request bits are effected.