R9A06G062GNP

R35AN0013EJ0100
Rev.1.00
Mar. 14, 2022

Design Guidelines for Circuit Boards with the Sub-GHz Transceiver

Summary

This application note gives guidelines for designing circuit boards that incorporate the R9A06G062GNP.

Target Device

R9A06G062GNP

Contents

1. Introduction

This application note gives guidelines for designing circuit boards that incorporate the R9A06G062GNP. The RTK0EE0012D01001BJ evaluation kit with the R9A06G062GNP and F2977 SPDT RF switch is used as an example.

Caution Descriptions in this application note are examples for reference. Following the guidelines does not guarantee the quality of characteristic signals. In attempting to use this device in your actual system, extensively consider and evaluate the system as a whole. Choosing to use the device in your system is at your own responsibility.

1.1 Related Document

Also refer to the following document related to this application note.

R9A06G062GNP Sub-GHz Transceiver User's Manual: Hardware

1.2 Reference Diagram of Circuits

Figure 1 - 1 is a diagram of circuits of the RTK0EE0012D01001BJ evaluation kit for reference.

Figure 1 - 1 Diagram of Circuits of the RTK0EE0012D01001BJ Evaluation Kit for Reference

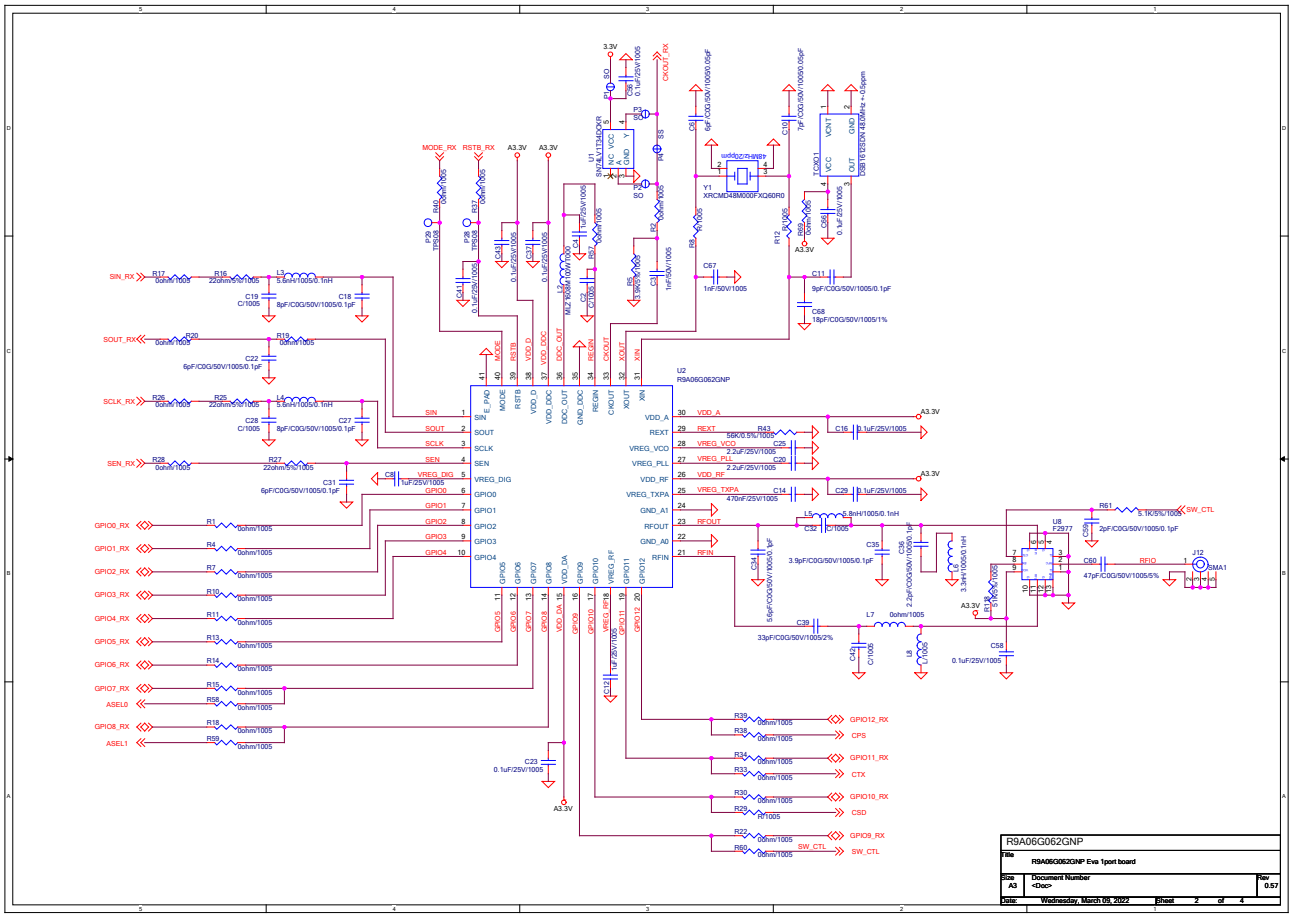


Table 1 - 1 lists components in the reference diagram of circuits shown in Figure 1 - 1.

Table 1 - 1 Components in the Reference Diagram of Circuits (Figure 1 - 1)

Part Reference	Description	Part Number	Vendor	Package Size (mm)	Tolerance
C3, C67	1nF/50V/1005	GCM155R71H102KA37D	Murata	1005	±10%
C4, C8, C12	1µF/25V/1005	GRM155R61E105KA12D	Murata	1005	±10%
C6	6pF/C0G/50V/1005/0.05pF	GJM1555C1H6R0WB01D	Murata	1005	±0.05 pF
C10	7pF/C0G/50V/1005/0.05pF	GJM1555C1H7R0WB01D	Murata	1005	±0.05 pF
R12	22nH/350mA/1005	LQG15HS22NJ02D	Murata	1005	±5%
C11	9pF/C0G/50V/1005/0.1pF	GJM1555C1H9R0BB01D	Murata	1005	±0.1 pF
C14	470nF/25V/1005	GRM155R61H474KE11D	Murata	1005	±10%
C16, C23, C29, C37, C41, C43, C45, C47, C48, C49, C50, C51, C52, C53, C54, C55, C56, C58, C66, C201	0.1µF/25V/1005	GRM155R71E104KE14D	Murata	1005	±10%
C18, C27	8pF/C0G/50V/1005/0.1pF	GJM1555C1H8R0BB01D	Murata	1005	±0.1 pF
C20, C25	2.2µF/25V/1005	GRM155R61E225KE11D	Murata	1005	±10%
C22, C31	6pF/C0G/50V/1005/0.1pF	GJM1555C1H6R0BB01D	Murata	1005	±0.1 pF
C34	5.6pF/C0G/50V/1005/0.1pF	GJM1555C1H5R6BB01D	Murata	1005	±0.1 pF
C35	3.9pF/C0G/50V/1005/0.1pF	GJM1555C1H3R9BB01D	Murata	1005	±0.1 pF
C36	2.2pF/C0G/50V/1005/0.1pF				
C39	33pF/C0G/50V/1005/2%	GJM1555C1H330GB01D	Murata	1005	±2%
C46	4.7µF/X7R/25V/2125	C2012X7R1E475K125AB	TDK	2125	±10%
C59	2pF/C0G/50V/1005/0.1pF	GJM1555C1H2R0BB01D	TDK	1005	±0.1 pF
C60	47pF/C0G/50V/1005/5%	GJM1555C1H470JB01D	TDK	1005	±5%
C68	18pF/C0G/50V/1005/1%	GCM1555C1H180FA16D	Murata	1005	±1%
L2	MLZ1608M100WT000	MLZ1608M100WT000	TDK	1608	±20%
L3, L4	5.6nH/1005/0.1nH	LQW15AN5N6C10D	Murata	1005	±0.1 nH
L5	5.8nH/1005/0.1nH	LQW15AN5N8B00D	Murata	1005	±0.1 nH
L6	3.3nH/1005/0.1nH	LQW15AN3N3B80D	Murata	1005	±0.1 nH
R1, R2, R4, R7, R10, R11, R13, R14, R15, R17, R18, R19, R20, R22, R26, R28, R30, R33, R34, R37, R38, R39, R40, R57, R58, R59, R60, R62, R69, L7	0ohm/1005	RK73Z1ETTP	KOA	1005	< 50 mohms
R5	3.9K/5%/1005	RK73B1ETTP392J	KOA	1005	±5%
R16, R25, R27	22ohm/5%/1005	RK73B1ETTP220J	KOA	1005	±5%
R8, R29, R44, R201, R202, R203, R204, R205, R206	R/1005				
R43	56K/0.5%/1005	ERA-2AED563X	Panasonic	1005	±0.5%
R45, R46, R47, R48, R49, R51, R61	5.1K/5%/1005	RK73B1ETTP512J	KOA	1005	±5%
R50, R54	10K/5%/1005	RK73B1ETTP103J	KOA	1005	±5%
R52, R53, R55, R118	51K/5%/1005	RK73B1ETTP513J	KOA	1005	±5%
R56	1K/5%/1005	RK73B1ETTP102J	KOA	1005	±5%
R207, R208, R209, R210, R211, R212	33ohm/5%/1005	RK73B1ETTP330J	KOA	1005	±5%
TCXO1	DSB1612SDN 48.0MHz ±0.5ppm	DSB1612SDN 48.0MHz ±0.5ppm	KDS		
U1	SN74LV1T34DCKR	SN74LV1T34DCKR	TI		
U2	R9A06G062GNP	R9A06G062GNP	Renesas		
U8	F2977	F2977NEGK	Renesas/IDT		
Y1	XRCMD48M000FXQ60R0	XRCMD48M000FXQ60R0	Murata	1612	±20 ppm

1.3 RF Matching Circuits

1.3.1 Transmitted output matching circuit

Figure 1 - 2 shows an example of the configuration of a transmitted output matching circuit. We recommend adding a notch filter circuit following the LC filter in the line from the RFOUT pin (pin 23). This is to suppress the second higher harmonic component from the fundamental waveform. Table 1 - 2 lists examples of the constants for the transmitted output matching circuit.

Figure 1 - 2 Example of the Configuration of a Transmitted Output Matching Circuit

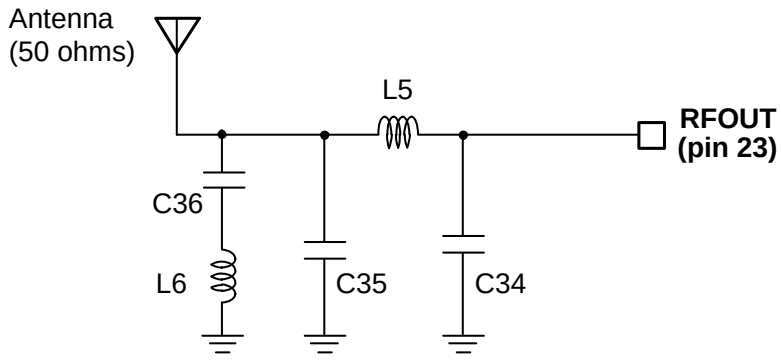


Table 1 - 2 Examples of the Constants for the Transmitted Output Matching Circuit

Component	C34	L5	C35	L6	C36
Value	5.6 pF	5.8 nH	3.9 pF	3.3 nH	2.2 pF

1.3.2 Received input matching circuit

Figure 1 - 3 shows an example of the configuration of a received input matching circuit. We recommend impedance matching at 50 ohms for the received input. Table 1 - 3 lists examples of the constants for the received input matching circuit.

Figure 1 - 3 Example of the Configuration of a Received Input Matching Circuit

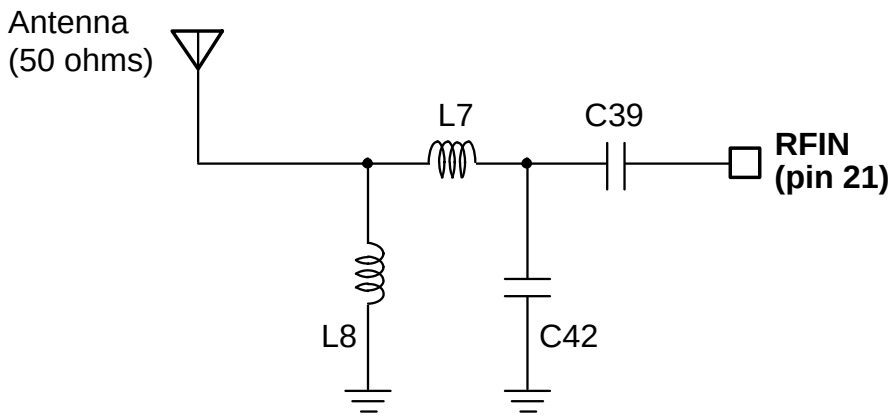


Table 1 - 3 Examples of the Constants for the Received Input Matching Circuit

Component	C39	L7	C42	L8
Value	33 pF	0 ohms	Not mounted	Not mounted

1.4 RF Input/Output Circuits

Figure 1 - 4 shows an example of the connection of the F2977 SPDT RF switch to the RF input/output circuits. Table 1 - 4 lists examples of the constants for the circuits shown in Figure 1 - 4. Table 1 - 5 shows an example of the connection of the F2977 SPDT RF switch in the RF signal lines.

Figure 1 - 4 Example of the Connection of the F2977 SPDT RF Switch to the RF Input/Output Circuits

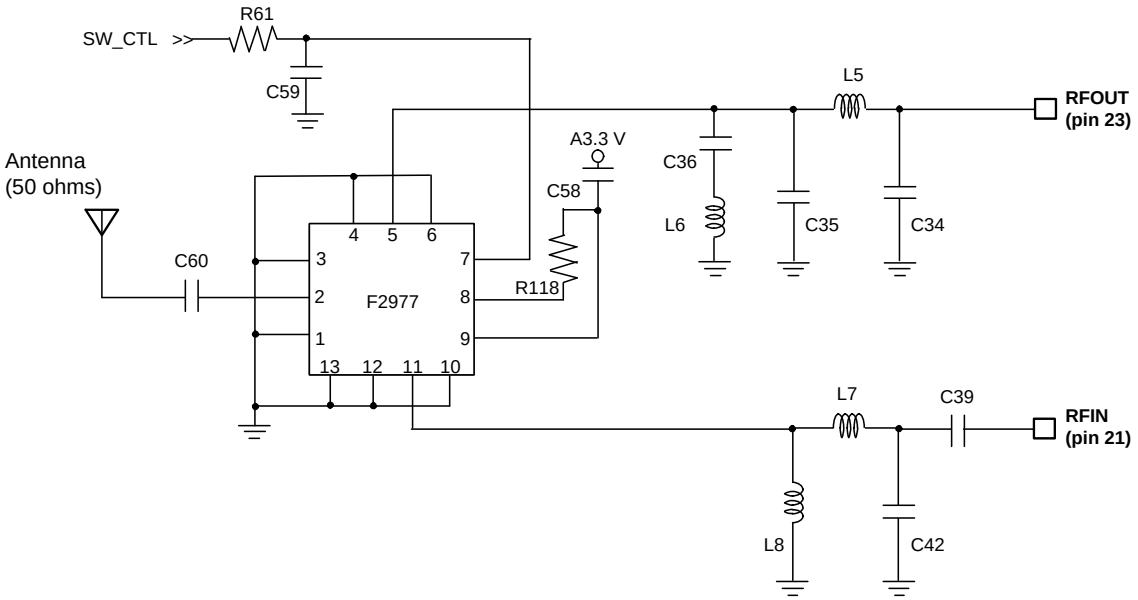


Table 1 - 4 Components and Examples of the Constants for the RF Input/Output Circuits with the F2977 SPDT RF Switch in Figure 1 - 4

Component ID	Component Value
R61	5.1 Kohms
C59	2 pF
C60	47 pF
R118	51 Kohms
C58	0.1 µF
C39	33 pF
L7	0 ohms
C42	Not mounted
L8	Not mounted
C34	5.6 pF
L5	5.8 nH
C35	3.9 pF
L6	3.3 nH
C36	2.2 pF

Table 1 - 5 Example of the Connection of the F2977 SPDT RF Switch in the RF Signal Lines

Pin No.	Pin Name	Description	Destination for Connection
1	GND	Ground pin	Ground
2	RFC	RF common port pin	Antenna (50-ohm load)
3	GND	Ground pin	Ground
4	GND	Ground pin	Ground
5	RF1	RF1 port pin	Pin 23 (RFOUT) of the R9A06G062GNP
6	GND	Ground pin	Ground
7	Vcn	Logic control pin	Pin 16 (GPIO9) of the R9A06G062GNP
8	EN	Active-high enable pin	A3.3 V power supply
9	Vcc	Power supply pin	A3.3 V power supply
10	GND	Ground pin	Ground
11	RF2	RF2 port pin	Pin 21 (RFIN) of the R9A06G062GNP
12	GND	Ground pin	Ground
13	Exposed pad	Exposed pad pin	Ground

1.5 Reference Clock Circuits

1.5.1 Using a 48-MHz crystal oscillator

Figure 1 - 5 shows an example of the standard configuration with a crystal oscillator. Ensuring stable oscillation by the 48-MHz crystal oscillator requires inserting a capacitor in the lines from each of the XIN (pin 31) and XOUT (pin 32) pins. We also recommend inserting an inductor in series between the XIN pin (pin 31) and the crystal resonator to suppress the harmonic components from the 48-MHz oscillation. Note that inserting either a resistor or inductor as R12 and R8 may be required in response to the state of the spurious emissions from this clock signal.

Table 1 - 6 lists examples of the constants for the crystal oscillator with the use of the XRCMD48M000FXQ60R0 from Murata as a crystal resonator (Y1). Before final determination of the constants, we recommend you proceed with sufficient evaluation from the various relevant viewpoints, such as the type of crystal resonator and the stray capacitance generated by the patterns for your own PCB.

Figure 1 - 5 Example of the Configuration of the Crystal Oscillator

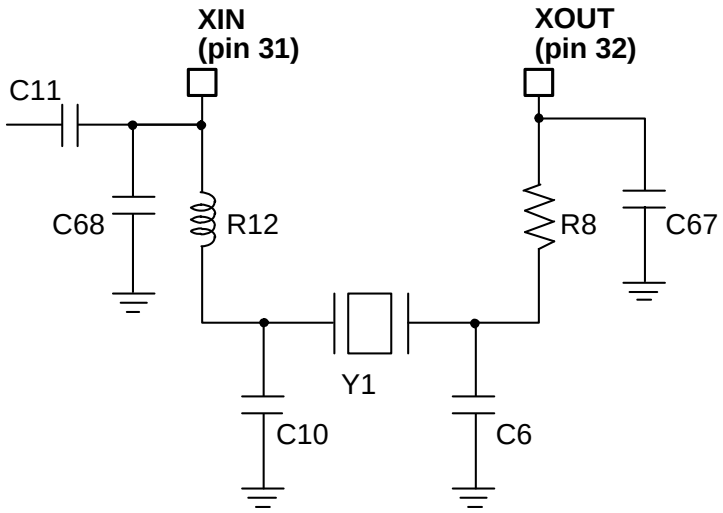


Table 1 - 6 Examples of the Constants for the Crystal Oscillator When Using the XRCMD48M000FXQ60R0 from Murata as Crystal Resonator Y1

Component ID	Component Value
C6	6 pF
C10	7 pF
C11	Not mounted
C67	Not mounted
C68	Not mounted
R8	0 ohms
R12	22 nH

1.5.2 Using a 48-MHz TCXO

Figure 1 - 6 shows an example of the standard configuration of a circuit with the use of a temperature-compensated crystal oscillator (TCXO). To suppress the harmonic components, we recommend adjusting the voltage amplitude value of output from the 48-MHz TCXO, input of a signal to the XIN pin (pin 31), and inserting a capacitor in the line from the XOUT pin (pin 32).

Table 1 - 7 lists typical values of the constants for the circuit with the use of the DSB1612SDN from KDS as the TCXO. Before final determination of the constants, we recommend you proceed with sufficient evaluation from the various relevant viewpoints, such as the type of TCXO and the stray capacitance generated by the patterns for your own PCB.

Figure 1 - 6 Example of the Configuration of a Circuit with the Use of a TCXO

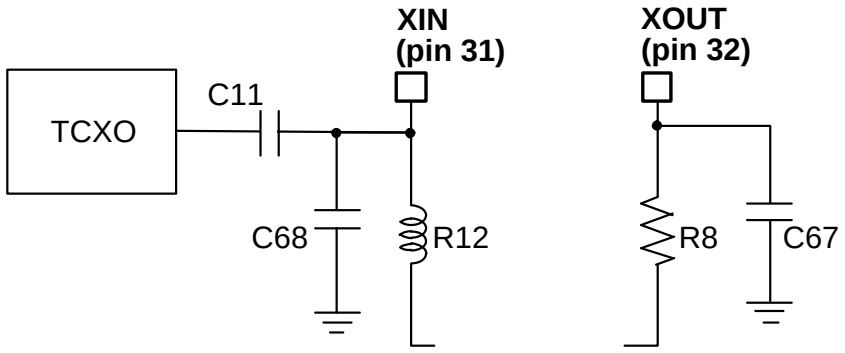


Table 1 - 7 Examples of the Constants for the TCXO Circuit When Using the DSB1612SDN from KDS as the TCXO

Component ID	Component Value
C68	18 pF
C11	9 pF
C67	1 nF
R8	Not mounted
R12	Not mounted

1.6 Circuit for Connecting the Serial Peripheral Interface (SPI)

Figure 1 - 7 shows an example of the circuit configuration around the SPI. The R9A06G062GNP has the SIN (pin 1), SOUT (pin 2), SCLK (pin 3), and SEN (pin 4) pins for the SPI signals. The R9A06G062GNP is connected with the external master microcontroller and operates as a slave device. Some transfer rates for the SPI may lead to the harmonic components at integer multiples of the SCLK signal frequency adversely affecting the operation within the desired bandwidth. We recommend inserting damping resistors or low-pass filters for suppressing the harmonic components in response to the state of the spurious emissions from the SCLK signal for the SPI.

Table 1 - 8 lists examples of the constants for the circuit when the clock signal for communications is at 24 MHz.

Figure 1 - 7 Example of the Circuit Configuration around the SPI

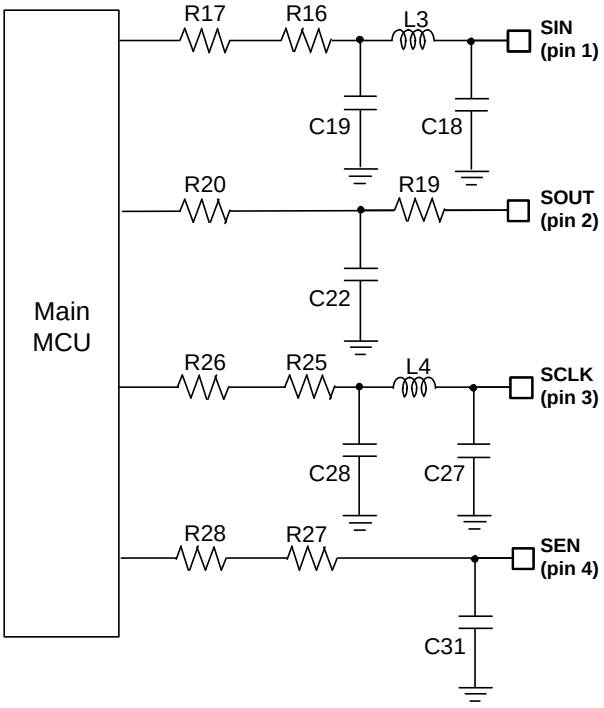


Table 1 - 8 Examples of the Constants for the Circuit When the SPI Clock Signal Is at 24 MHz

Component ID	Component Value
C18	8 pF
C19	Not mounted
L3	5.6 nH
R16	20 ohms
R17	0 ohms
R19	0 ohms
R20	0 ohms
C22	6 pF

Component ID	Component Value
C27	8 pF
C28	Not mounted
L4	5.6 nH
R25	22 ohms
R26	0 ohms
C31	6 pF
R27	22 ohms
R28	0 ohms

1.7 Circuit for the DC-DC Converter

Figure 1 - 8 shows an example of the external circuit configuration for the DC-DC converter. An additional LC low-pass filter in the line including R57 and C2 or connecting a ferrite bead to R57 may be required in response to the introduction of noise from operation of the DC-DC converter. Connect the grounds for capacitors C2 and C4 to the GND_DDC pin (pin 35) along the shortest possible paths.
Table 1 - 9 lists examples of the constants for the DC-DC converter circuit.

Figure 1 - 8 Example of the External Circuit Configuration for the DC-DC Converter

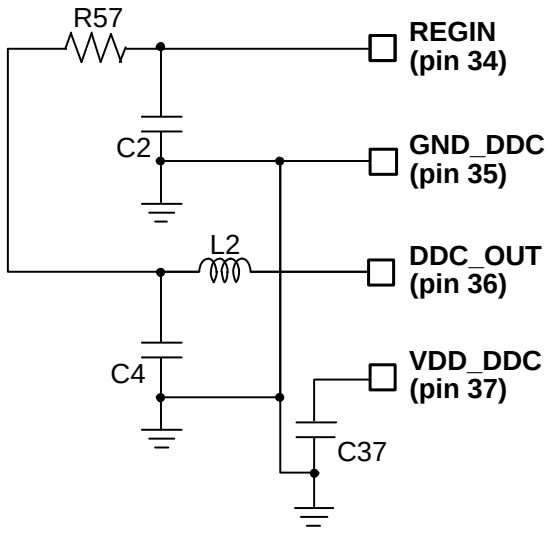


Table 1 - 9 Examples of the Constants for the DC-DC Converter Circuit

Component ID	Component Value
L2	10 µH
C4	1 µF
R57	0 ohms
C2	Not mounted
C37	0.1 µF

2. Design of the Pattern Layout of the Board

We recommend the application of the same principles for the pattern layout of a board as those applied on the evaluation board from Renesas.

As is the case with the evaluation board from Renesas, a PCB with four wiring layers is recommended.

- PCB material: FR-4
  Board thickness: 1.6 mm
  Number of layers: Four
- Major layer configuration (main intended use)
  First layer: signal lines, second layer: ground, third layer: VDD, forth layer: ground, signal lines, or ground and signal lines

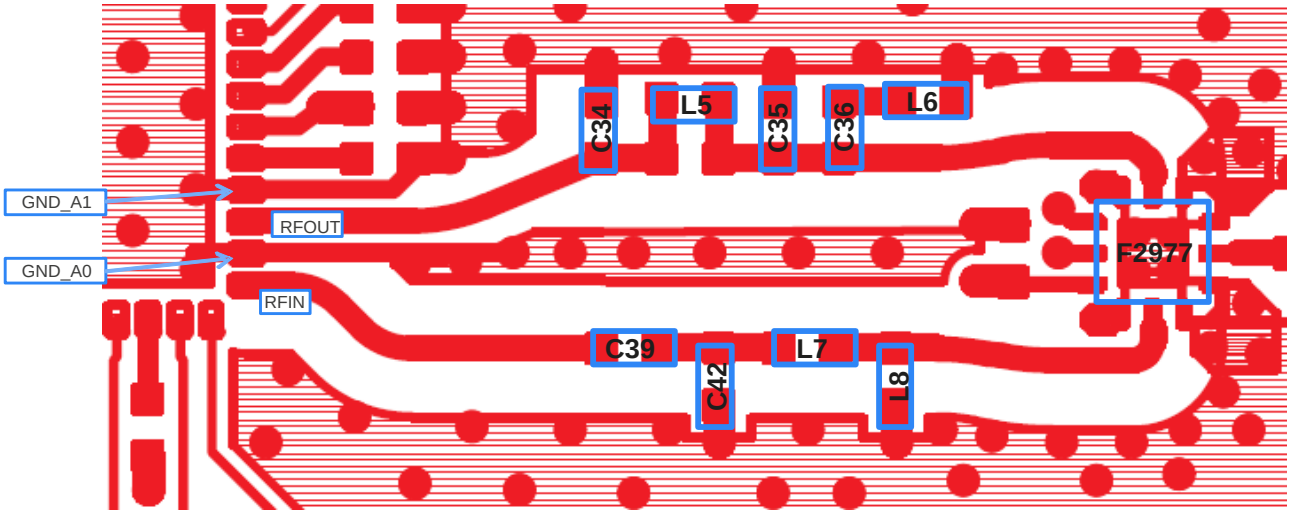
2.1 RF Input/Output Signal Lines

Points to note in the design of the wiring patterns around the RF input/output signal lines are as follows.

- Use microstrip lines for the RF signals and design the wiring patterns to maintain characteristic impedances of 50 ohms.
- Place as many via holes as possible around the microstrip lines and secure the widest possible ground regions. Also secure the widest possible ground regions and do not place the lines for different signals in the second layer just below the RF signal lines.
- Secure the widest possible ground regions for the GND_A0 (pin 22) and GND_A1 (pin 24) pins. Connect these pins to the ground pad just below the IC in the surface layer along the shortest possible paths and connect the pins to the ground (second) layer through as many via holes as possible, and such that the wiring lengths become as short as possible.

Figure 2 - 1 shows an example of the wiring patterns around the RF signal lines.

Figure 2 - 1 Examples of Layout of the Patterns around the RF Signal Lines



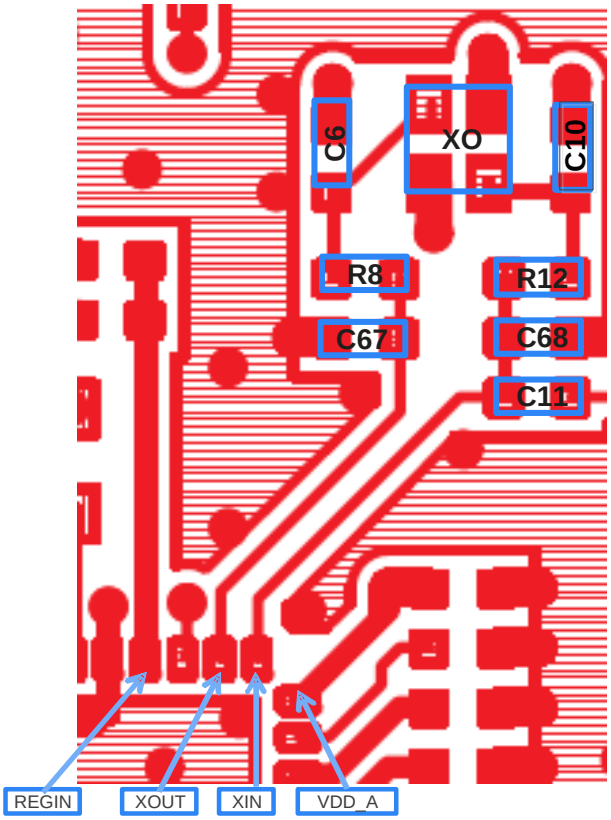
2.2 Crystal Oscillator

Points to note in the design of the wiring patterns for the crystal oscillator are as follows.

- Place capacitors C6 and C10 close to the electrodes of the crystal resonator.
- To avoid intermodulation, the wiring runs between the XIN (pin 31) and XOUT (pin 32) pins and the crystal resonator (Y1) should be at almost the same distance from the REGIN (pin 34) and VDD_A (pin 30) pins, respectively.
- Do not place signal lines other than those for the XIN and XOUT pins around the crystal resonator.
- Separate the grounds for the crystal resonator and capacitors C6 and C10 in the surface layer and connect the grounds to the ground (second) layer through via holes along the shortest possible paths.
- Proceed with sufficient evaluation of your system in detail before determining the constants for the circuits related to the crystal resonator.
- Inductors may be inserted as R12 and R8 as required in response to the spurious emissions from clock signals with frequencies of 864 MHz and 912 MHz, both integer multiples of the crystal frequency (48 MHz), for channels in the vicinity of the oscillator. We recommend mounting a 22-nH inductor as R12, as is the case on the evaluation board from Renesas.

Figure 2 - 2 shows an example of the layout of wiring patterns related to the crystal resonator.

Figure 2 - 2 Example of Layout of Wiring Patterns around the Crystal Resonator



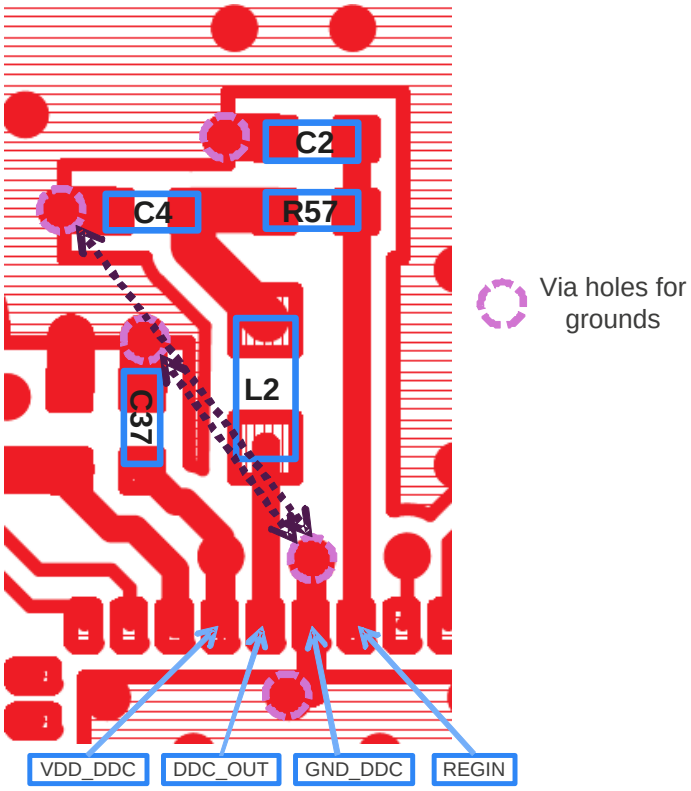
2.3 DC-DC Converter Circuit

Points to note in the design of the feedback loop patterns for the output line of the DC-DC converter are as follows.

- Do not place signal lines around the REGIN (pin 34), GND_DDC (pin 35), DDC_OUT (pin 36), and VDD_DDC (pin 37) pins.
- Make the wiring loop between the REGIN and DDC_OUT pins as short as possible.
- Place capacitor C37 as close as possible to the VDD_DDC pin.
- Place grounds for capacitors C4 and C37 such that they can be connected to the GND_DDC pin along the shortest possible paths on the ground surface.
- An additional LC low-pass filter in the line including R57 and C2 or connecting a ferrite bead to R57 may be required in response to the introduction of noise from operation of the DC-DC converter.

Figure 2 - 3 shows an example of the layout of wiring patterns around the DC-DC converter circuit.

Figure 2 - 3 Example of Layout of Wiring Patterns for the DC-DC Converter Circuit



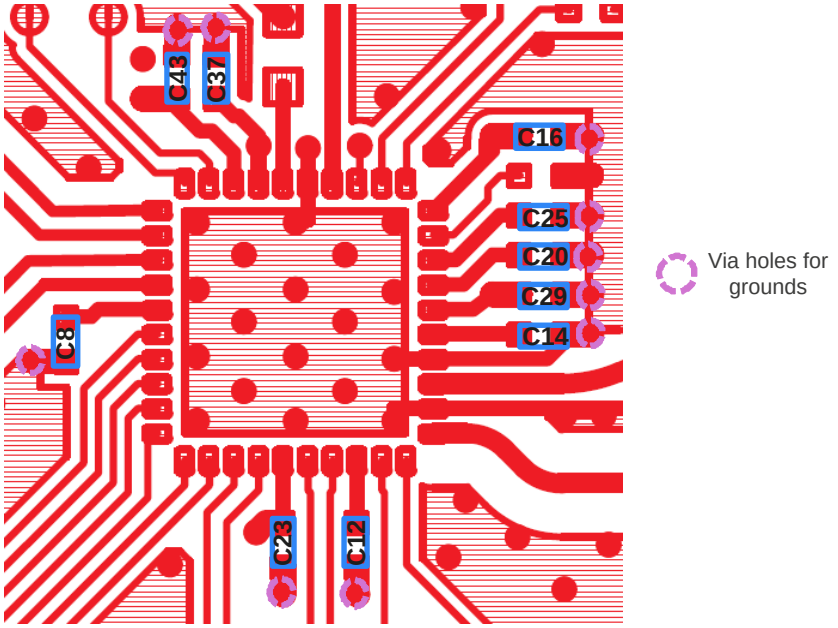
2.4 Power Supplies

Points to note in the design of the pattern layouts for power supplies on the board are as follows.

- Place bypass capacitors close to the respective power supply pins such that the wiring lengths are as short as possible.
- Place via holes for grounds close to grounds for the bypass capacitors such that the grounds can be connected to the ground (second) layer through the via holes along the shortest possible paths.
- Unless otherwise specified, keep wiring runs to power supply pins as thick as possible in consideration of keeping the impedances low.

Figure 2 - 4 shows an example of the layout of wiring patterns around power supplies.

Figure 2 - 4 Example of Layout of Wiring Patterns around Power Supplies



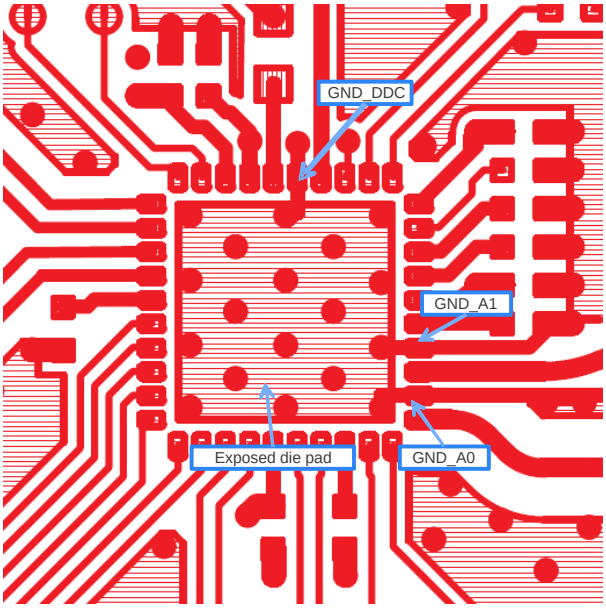
2.5 Grounds

Points to note in the design of the wiring patterns for grounds are as follows.

- Place as many via holes for grounds as possible.
- Use the second layer as the ground layer.
- Connect the GND_A0 (pin 22), GND_A1 (pin 24), and GND_DDC (pin 35) pins to the exposed die pad in the surface layer and connect them to the ground (second) layer through via holes along the shortest possible paths. Place many via holes on the exposed die pad.
- Do not place signal lines under the exposed die pad.

Figure 2 - 5 shows an example of the layout of wiring patterns around grounds.

Figure 2 - 5 Example of Layout of Wiring Patterns around Grounds



Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Mar. 14, 2022	—	First edition issued

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(Rev.5.0-1 October 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan

www.renesas.com

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General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.