Everywhere you imagine. RENESAS

Announcing the First Products in the RX MCU Family

Renesas Technology Corp.

March 25, 2009

Contents

Renesas Solutions in Response to Customer Requirements

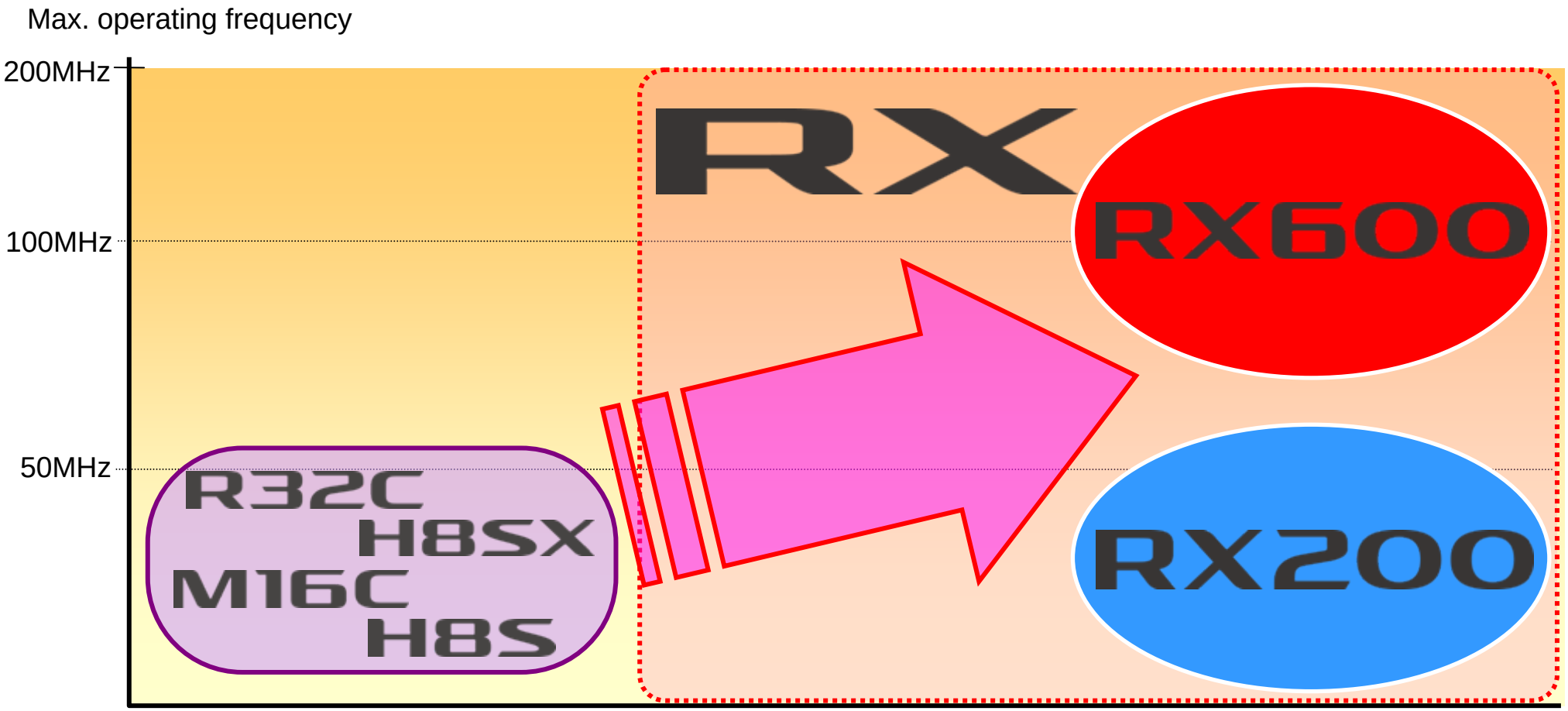
– Providing the world's fastest CISC MCUs: The RX Family –

Customer comment	Renesas solution
I want a CPU with better performance to deal with complex control tasks at high speed.	A CPU capable of 1.65 DMIPS/MHz, and speeds up to 200MHz. Leveraging CISC architecture to the fullest extent, RX code size is 30% smaller.
But I want to keep power consumption low.	RX MCUs available in two series to match application needs, balancing high performance with low power consumption. Core uses 0.03 mA/MHz
I want to reduce turnaround time by making use of design resources from existing products.	Ability to reuse software resources built for existing products

RX Family Series Evolution

- RX600 Series for high speed and extreme performance with low power consumption
- RX200 Series for high performance with ultra-low power consumption

➔ Responding to customer requirements.



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Key Features of RX CPU Core

1. Code efficiency
⇒Industry's highest code efficiency (30% better than existing Renesas products)

2. Excellent processing performance
⇒1.65 MIPS/MHz (approximately 2X performance of existing Renesas products)

3. Low power consumption
⇒CPU current consumption, 0.03 mA/MHz (1/3 of existing Renesas products)

4. Integrated Arithmetic Functions
⇒Floating Point, Multiply Accumulate (extremely efficient calculation and DSP)

Striving for Optimum Code Efficiency

- Extensive case study of many customer applications identified frequently used instructions, which were optimized and shortened

Enables more compact software code and use of products with less memory. (Example: Load/store instructions and compare instructions are two bytes shorter; branch instructions and add instructions are one byte shorter.)

- Byte-unit variable-length instructions

Instruction lengths range from one to eight bytes, and most frequently used instructions are less than four bytes. This increases storage granularity, wasting no memory space, and optimizes CPU fetching and execution of instructions.

- Additional addressing modes

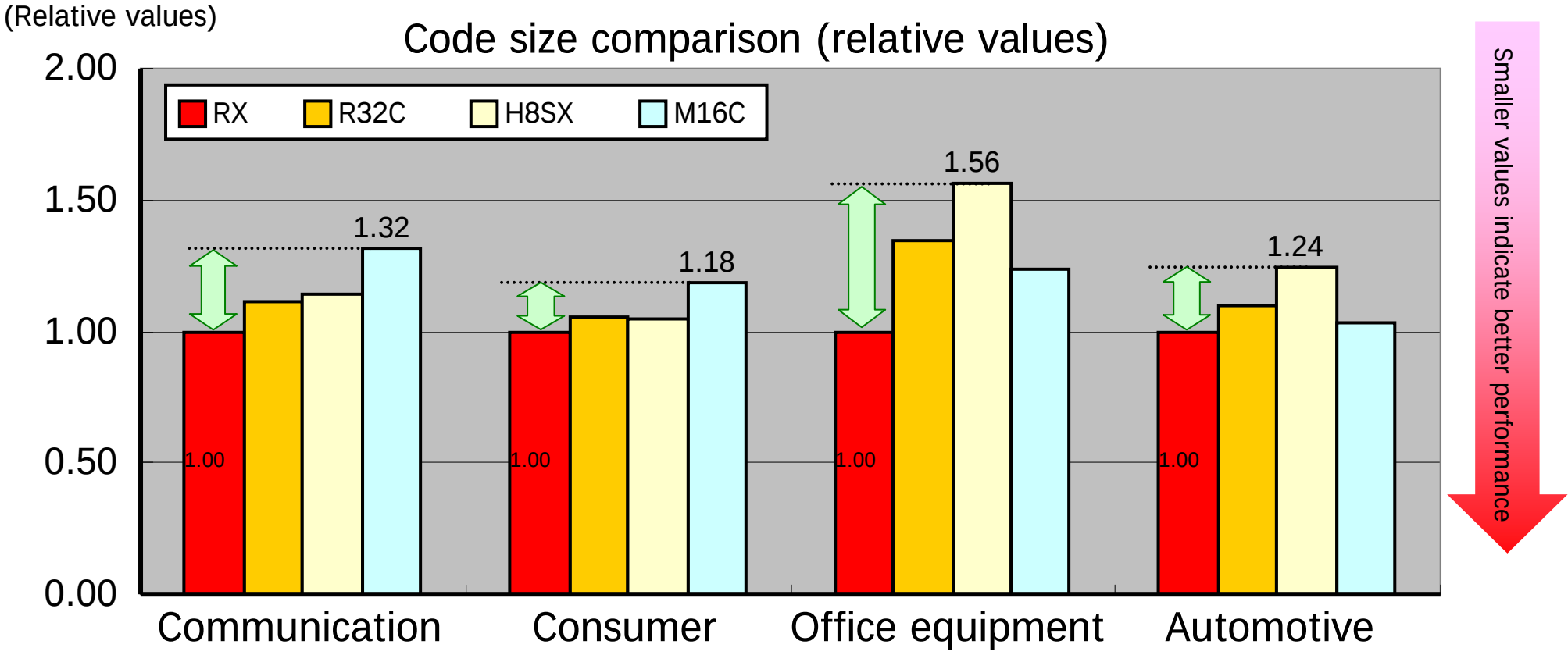
Much more efficient access and manipulation of tables, with smaller code size (post-increment/pre-decrement/indexed register indirect).

- Three-operand mode

Three registers can be specified at once, or one immediate and two registers for logic and arithmetic operations. Faster and smaller code (supports AND, OR, ADD, SUB, and MUL)

Code Size Efficiency: Benchmark Tests

- The RX CPU delivers 30% better code efficiency than existing products by optimizing the RX instructions, addressing modes, and compiler.



Note: Test results obtained using benchmarking software developed by Renesas Technology.

Excellent Processing Performance

- **Five-stage pipeline**

  Enables CPU to execute one instruction in just one clock when pipe is full

- **Harvard architecture**

  Enables simultaneous CPU access of both instructions and data to maximize the benefit of the five stage pipeline

- **Out-of-order instruction completion**

  Reduces the occurrence of empty “slots” in pipeline while an instruction is waiting for a pending result or action, maintaining one clock per instruction

- **Greatly improved DSP arithmetic functions**

  Single-cycle Multiply-Accumulate operates on coefficients in memory (32b x 32b to 80b result), or on coefficients in registers (16b x 16b to 48b result)

- **Single-precision floating-point unit**

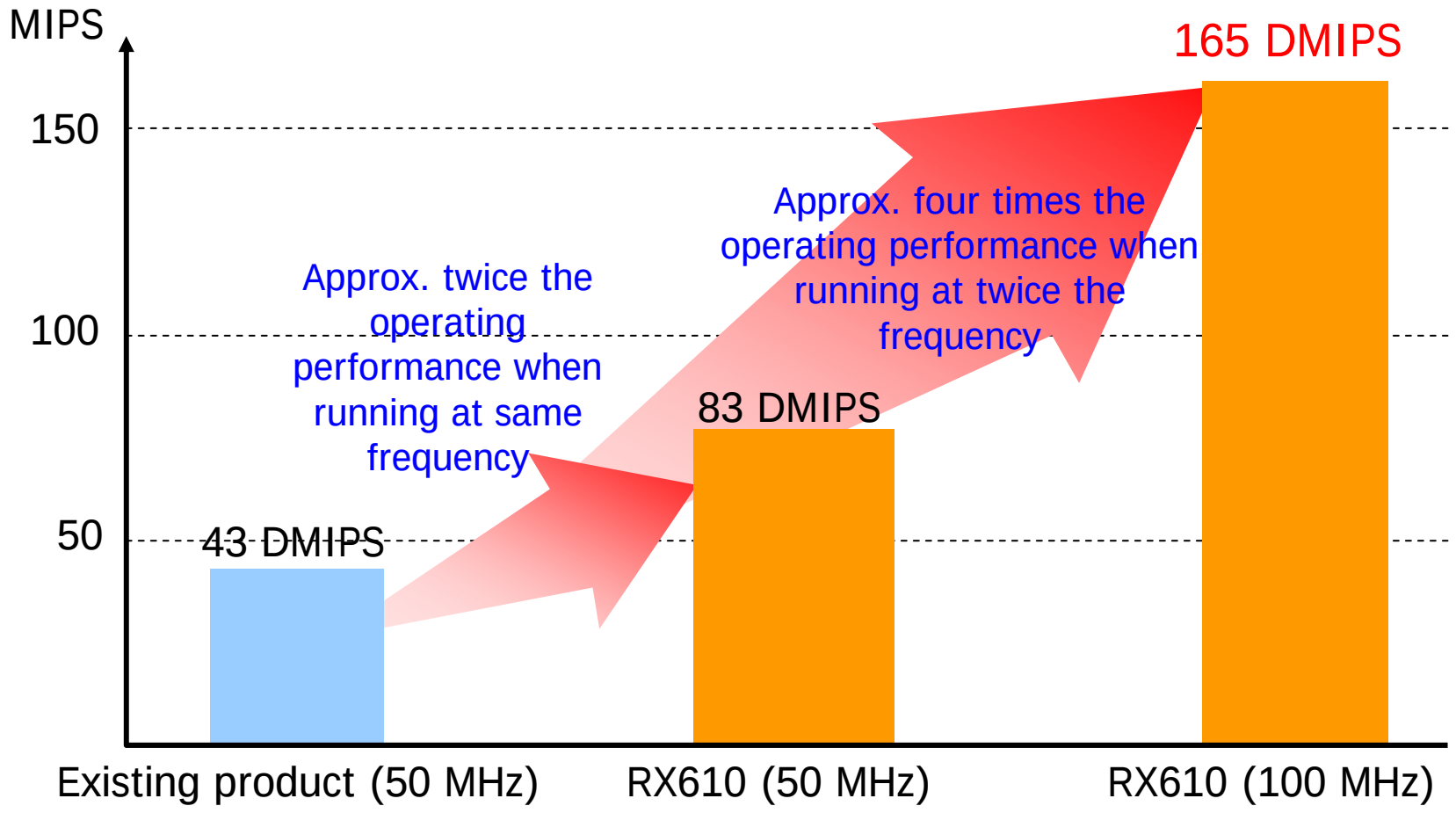
  No load/store operations required; arithmetic operations use general CPU registers directly for fastest possible results

- **Enhanced interrupt responsiveness**

  Interrupt latency as low as only five CPU clocks when using high-speed interrupts, ~50% improvement from previous products

Benchmark Tests (Dhrystone 2.1)

- The high-speed, high-performance RX CPU and optimized C compiler combine to deliver performance of 165 DMIPS when operating at 100 MHz.



Low Power Consumption

Clock gating design methodology

- The operation sequence is evaluated and supply of clock signal to unused blocks is cut off dynamically.
- Ultrafine 90 nm process node reduces load capacitance (gates, wiring).

Multi-threshold and minimal leakage current design methodology

- Basic design using low-leakage cells (high Vth) → Reduction of leakage current during normal operation
- Use of high-speed cells (low Vth) for critical paths → High-speed operation combined with low current consumption

Multiple Power Domains

- At MCU device level, the power to independent physical domains within the device may be shut off dynamically depending on which low power mode is being used, closely matching power consumption with tasks, with minimal waste

→ 0.03 mA/MHz for RX CPU core

Contents

Extending the EXREAL Concept to MCUs

Reliability
- Security
- High reliability

Efficiency
- Low power consumption
- Efficient development
- Continuity

Agility
- Better performance
- Realtime capabilities

High reliability for automotive applications
Low-noise/low-radiation technology

Low-power-consumption technology
Retention of peripheral circuits from previous MCUs
Shorter development cycles + easier evolution of new product versions

Integrated optimization of CPU, peripheral functions, and bus architecture for better performance and realtime capabilities

- Support for on-chip flash memory
- Support for various power supply and clock specifications

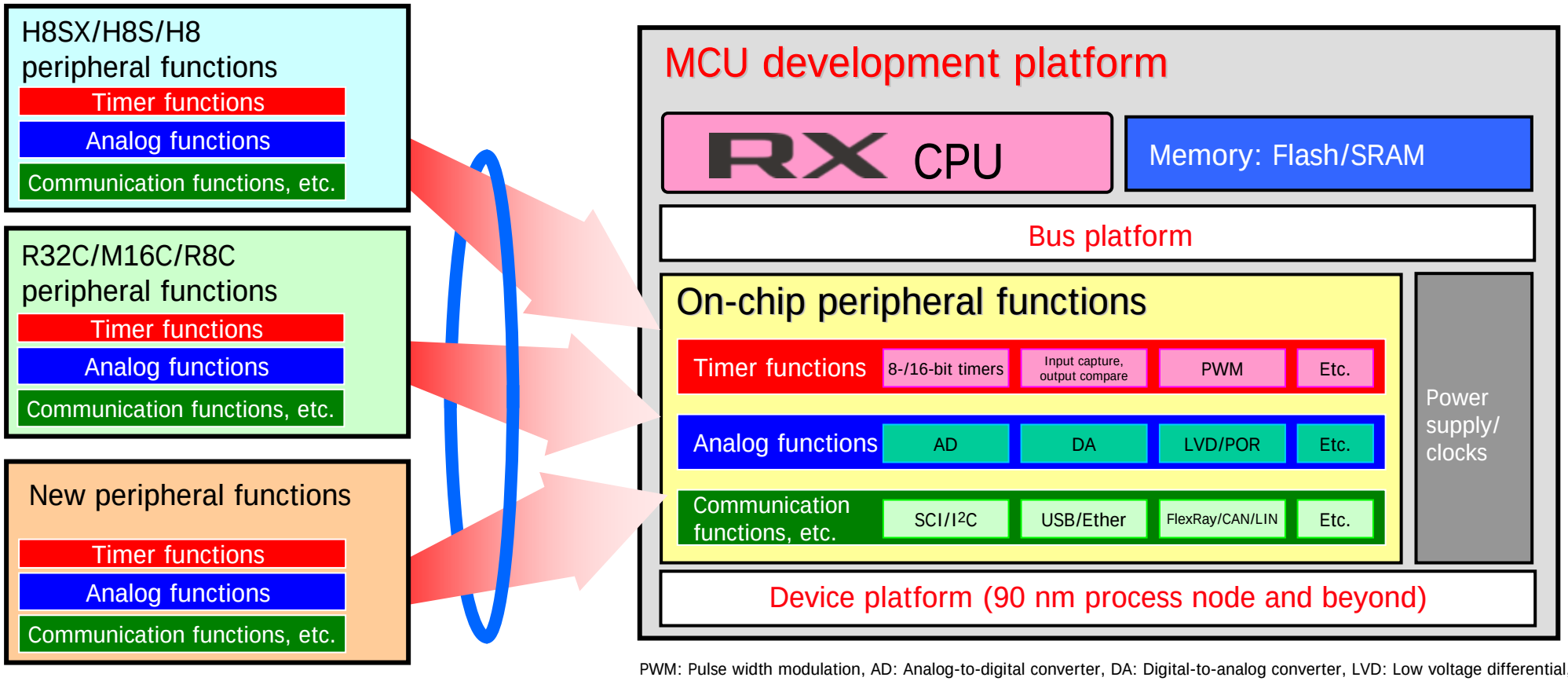
M16C
H8SX
H8S
R32C

MCU development platform

RX core + ♦ Design platform ♦ Device platform

Easy to Retain Peripheral Functions of Existing CPU Products and Add New Functions

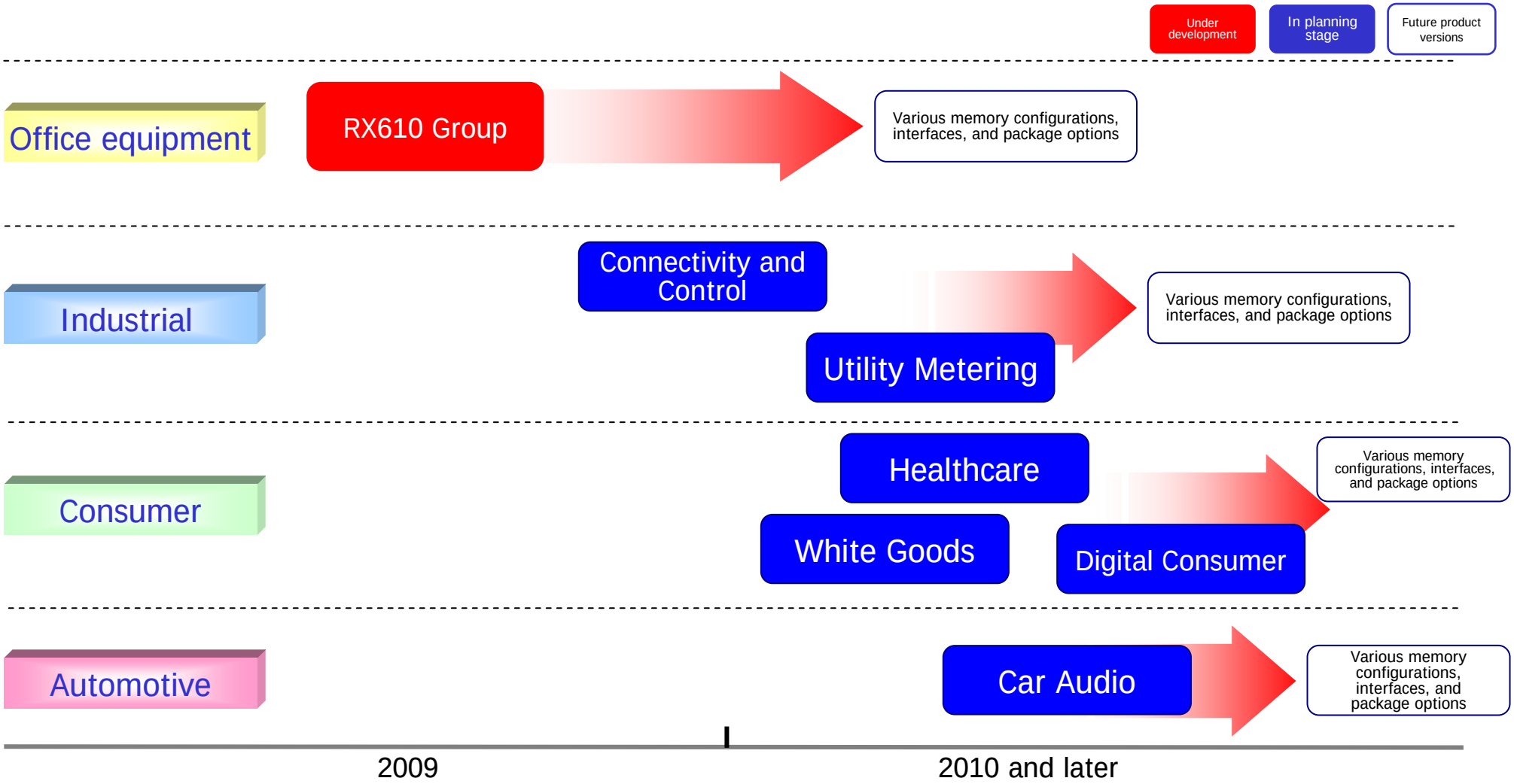
- Starting application of the MCU development platform with the RX Family
- Easy implementation of peripheral functions from existing products and new peripheral functions
  - → Prior development of peripheral functions for smooth product development (shorter TAT)
  - → Smooth development of products incorporating new functions and technologies (faster rollout horizontally)
  - → Smaller gaps between individual products for smoother portability (more flexibility)



PWM: Pulse width modulation, AD: Analog-to-digital converter, DA: Digital-to-analog converter, LVD: Low voltage differential, POR: Power-on reset, SCI: Serial communication interface; TAT: Turnaround time, I²C bus is a registered trademark of NXP B.V.

RX Family Product Roadmap

- MCU development platform is being utilized to start product development.



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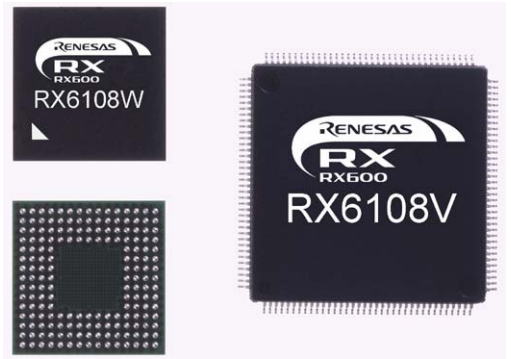
- Features of RX CPU Core
- MCU Development Platform
- Overview of First Products in RX Family
- Development Environment, Portability
- Conclusion



Features of First RX600 Products: RX610 Group

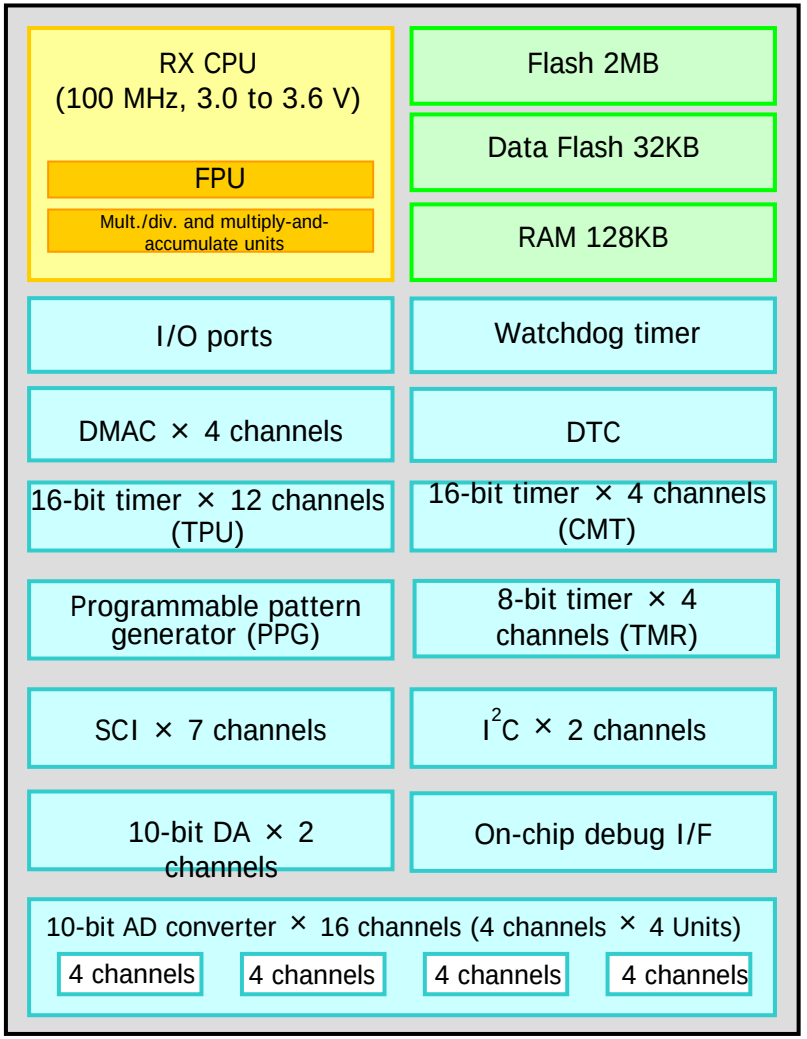
High speed, excellent performance	● Industry's top level of code efficiency (30% better than existing Renesas products) ● High processing speed of 165 DMIPS when operating at 100 MHz ● Hardware multiplier/divider, multiply-and-accumulate unit, and single-precision FPU for improved arithmetic performance
High speed, large-capacity on-chip memory	● Single-cycle access to flash memory when operating at 100 MHz ● Ample memory capacity — Flash: 2 MB, RAM: 128 KB ● 32 KB of on-chip data flash
Reduced current consumption	● Low current consumption of 50 mA when operating at 100 MHz ● Selectable power-down (low-power) modes to match various usage conditions
Full complement of peripheral functions	● Enhanced analog functions (high-speed 10-bit A/D, 10-bit D/A) ● Enhanced communication functions (SCI: 7 channels, I2C with Fast Mode Plus support) ● Full complement of timer modules (16-bit × 16 channels, 8-bit × 4 channels)
Continuity	● Maintains pin compatibility with M16C Family ● On-chip peripheral functions inherited from existing products
Debugging tools with advanced functions	● On-chip debugger with trace function (E1/E20) ● Full ICE support (E100 emulator)

RX610 Group RX6108 Product Overview

■ Built around the RX CPU core, the RX6108 provides large-capacity on-chip memory, many peripheral functions, and low current consumption.

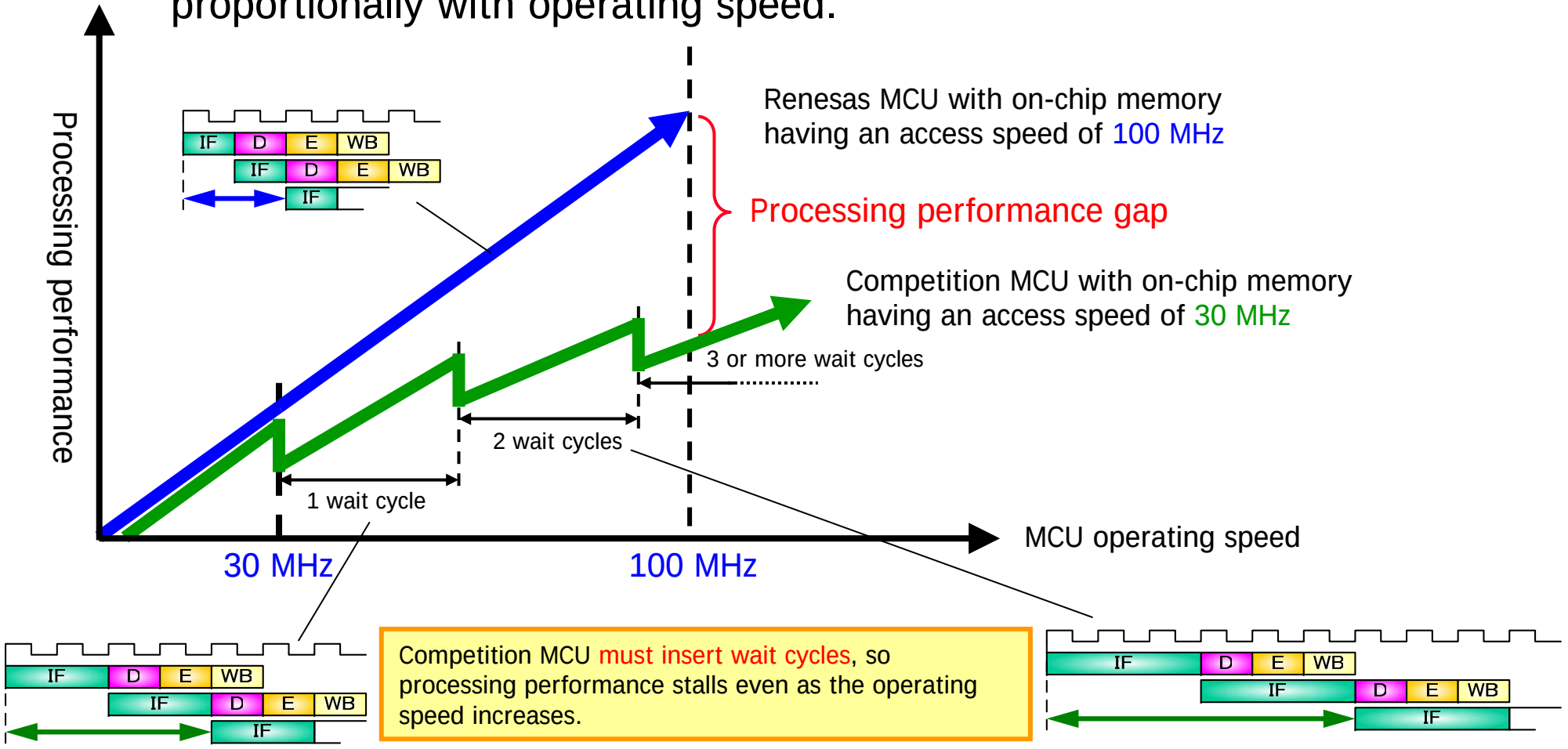
- High-speed operating frequency: 100 MHz
- High-performance RX CPU
  - High-speed operation: Basic instructions execute in 1 state (10 ns when operating at 100 MHz)
  - Arithmetic unit: 32-bit multiplier, divider, multiply-and-accumulate unit, FPU (single-precision)
- On-chip memory
  Program flash: 2 MB, data flash: 32 KB, RAM: 128 KB
- Peripheral functions
  - External bus extension function: 16-bit separate bus (ROM/RAM I/F, byte control SRAM I/F)
  - Transfer modules: DMAC, DTC
  - Timers
    Advanced-function general timer: 16-bit × 12 channels (TPU)
    Timer optimized to application or OS: 16-bit × 4 channels (CMT)
    General timer: 8-bit × 4 channels (TMR)
  - High-speed 10-bit A/D converter (conversion time: 1 μsec.)
  - 10-bit D/A converter: 2 channels
  - Communication functions
    Clock synchronous/asynchronous SCI × 7 channels
    I2C × 2 channels (Fast Mode Plus)
- Low current consumption: 50 mA when operating at 100 MHz
- Development environment
  - On-chip debug emulator
  - Full emulator
- Package
  - LQFP 144-pin, BGA 176-pin

RX6108 Product Block Diagram



High-Speed Large-Capacity Flash Memory

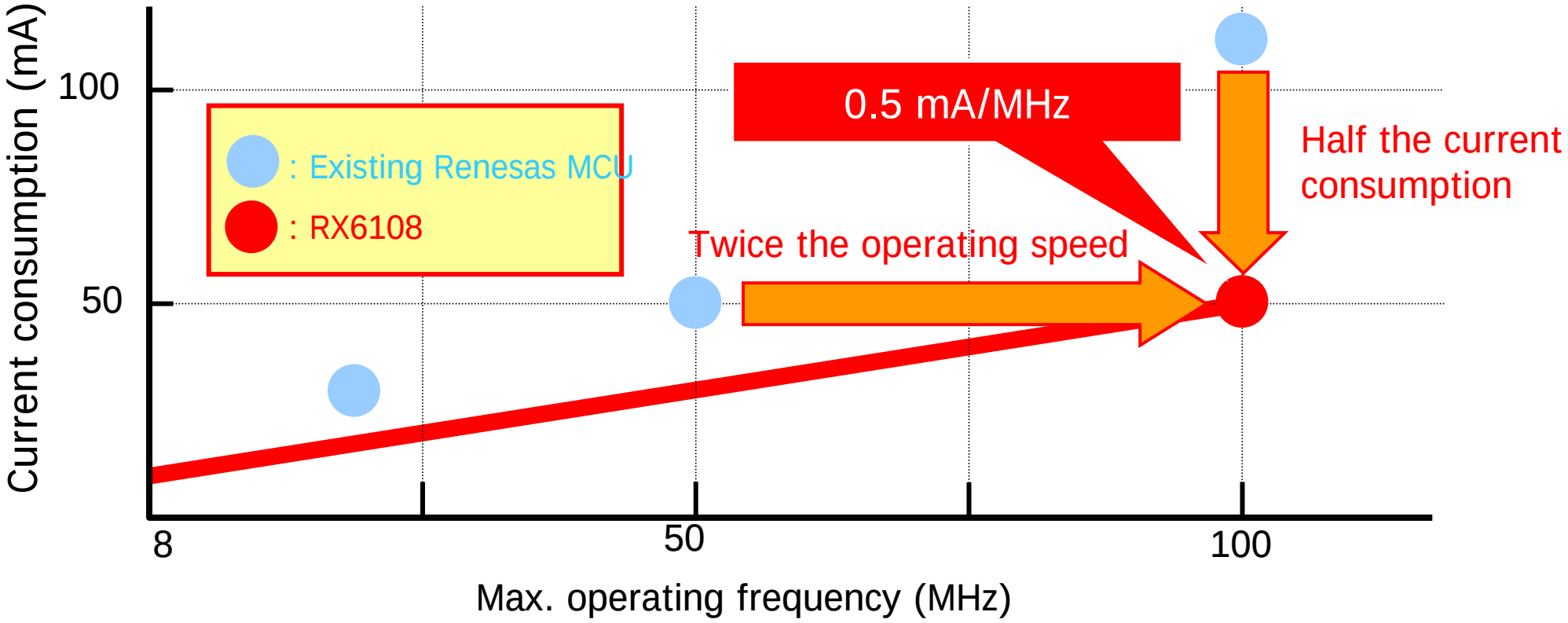
- Renesas achieves access speeds up to 100 MHz with no wait cycles
  - 100% of the RX CPU's performance potential is realized proportionally with operating speed.



Note: This example illustrates a case in which one wait cycle imposes overhead of 30%.

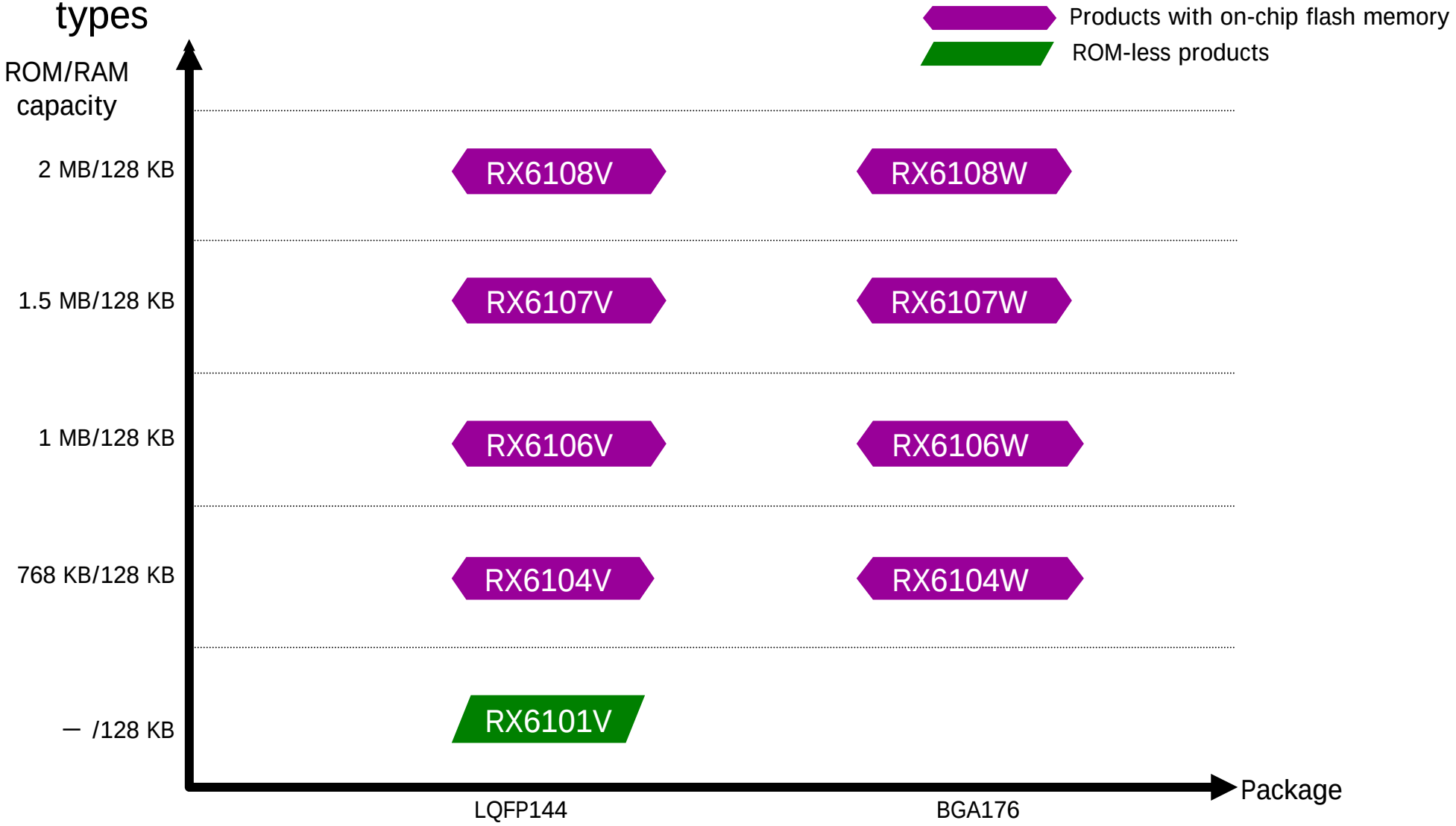
Low Current Consumption: Comparison with Existing Renesas MCU

- When operating at 100 MHz, the RX6108 achieves low current consumption of 50 mA, with all peripherals active.
  - Current consumption is halved when operating at the same frequency.
  - Operating speed is doubled at the same level of current consumption.



RX610 Group Product Lineup

- Eight products with different memory capacities and package types



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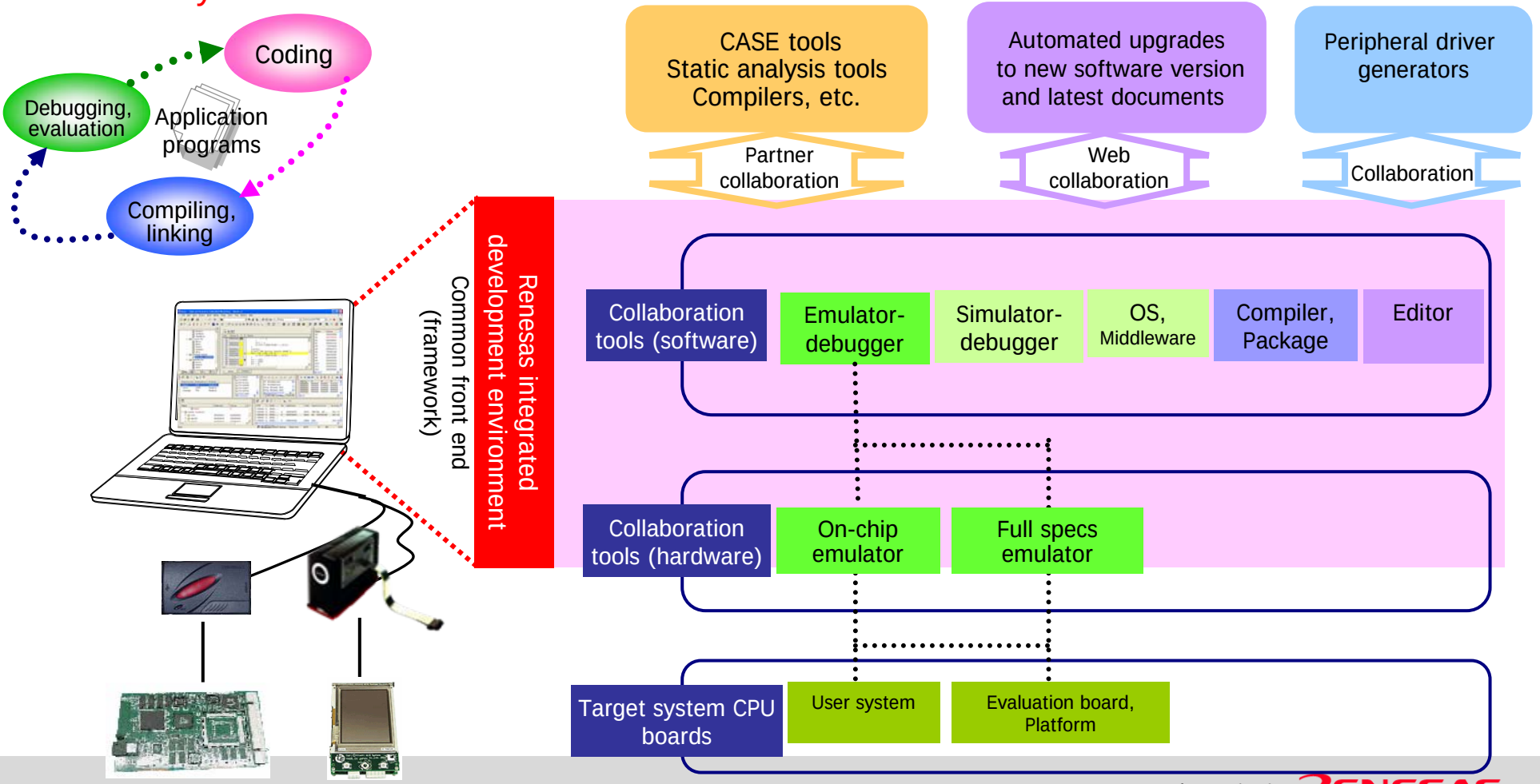
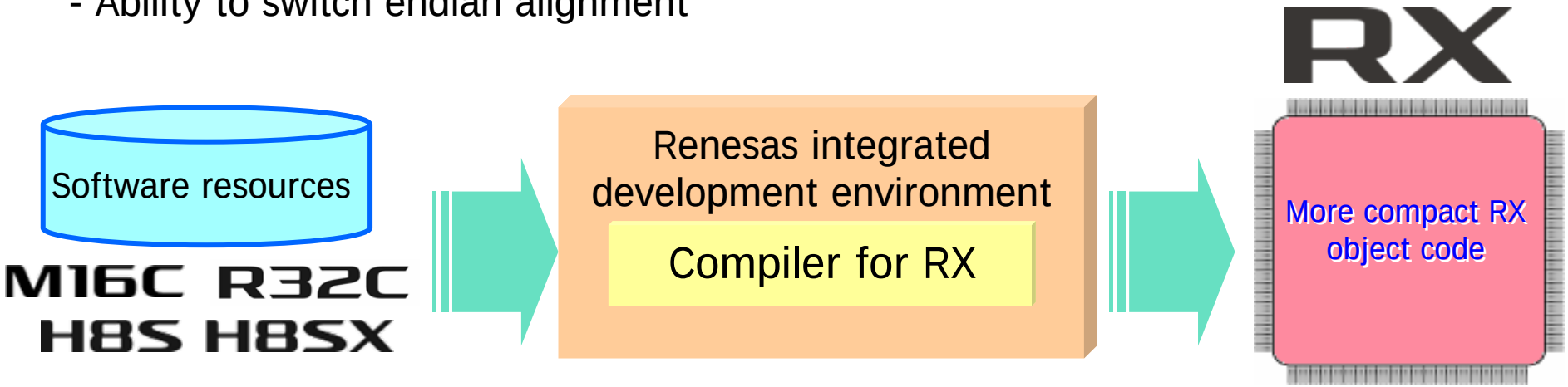
Continuation of Renesas Tool System

- The Renesas integrated development environment supports all stages of development.
- Internet-based services, driver generation tools for peripheral functions, etc., will continue to be available in the same way as existing products.
- Renesas is working with our partners to assure that a range of third party tools will be available for the RX family.



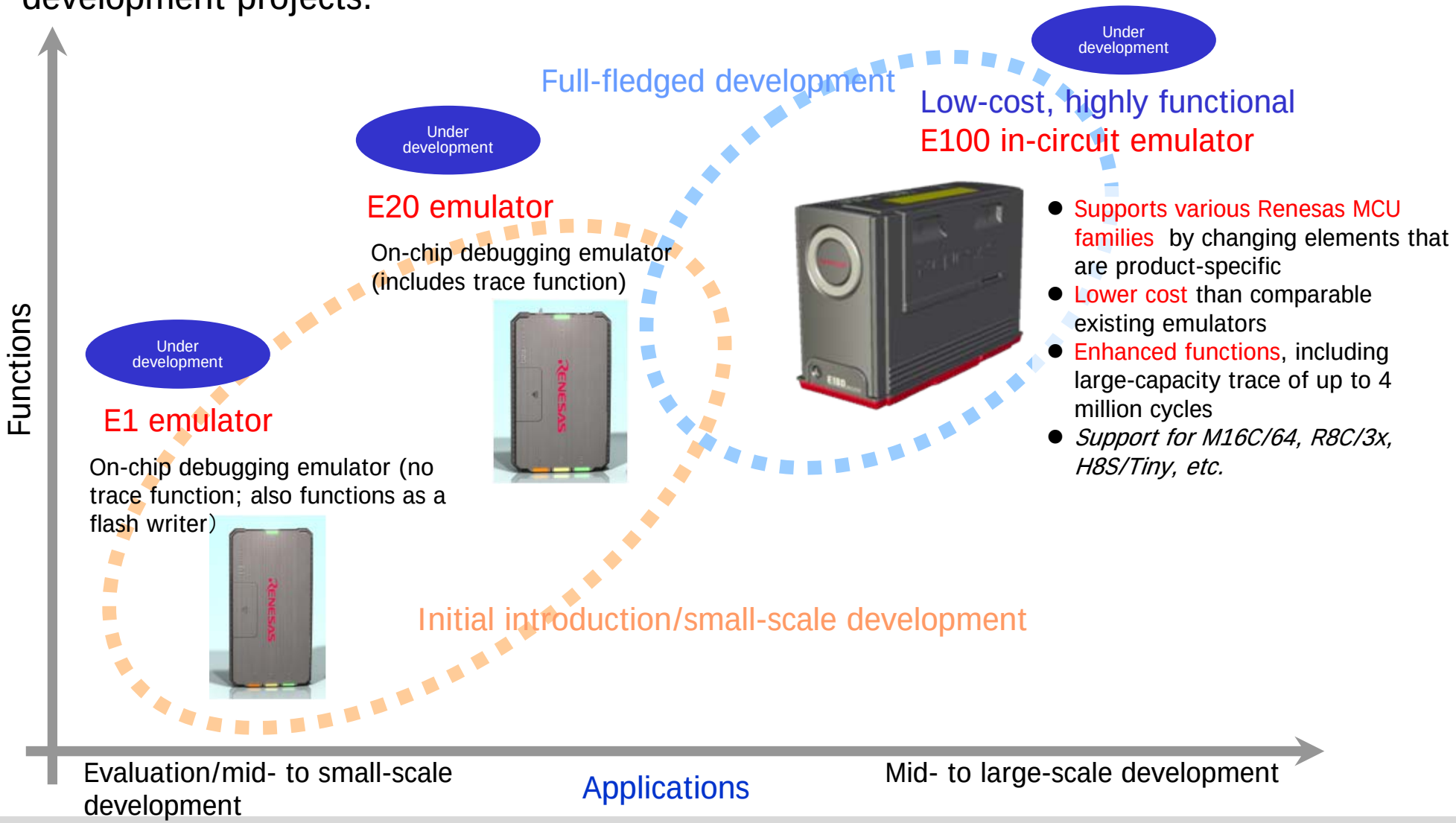
Improved C Compiler Optimization and Easier Porting of Software from Existing Products

- Better optimization for more compact code
  (Optimal register assignments, optimal instruction selection, instruction scheduling, etc.)
- Ability to easily port programs developed for existing Renesas products
  - Option settings that absorb language specifications
  - Checking of specific extended specifications
  - Ability to switch endian alignment



Emulator Lineup for RX610 Group

- RX emulator products provide support for small to large-scale development projects.



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Conclusion

- The RX610 Group is released as the first products in the RX Family.
- The RX CPU realizes industry-top-level code efficiency and delivers industry-top-class processing performance of 1.65 DMIPS/MHz.
- High-speed performance is supported by fast flash memory technology, one of Renesas Technology's strengths.
- Advanced 90 nm process node technology makes possible large-capacity on-chip memory and low power consumption while reducing the overall cost of the customer's system.
- Mass production plans: RX610 Group
  - Start of mass production: 1st half of 2010, 100,000 units/month
  - Stable period: 2011, 1 million units/month

Renesas Technology Corp.