

Everywhere you imagine. **RENESAS**



New Next-Generation CISC CPU "RX"

November 8, 2007

Renesas Technology Corp.

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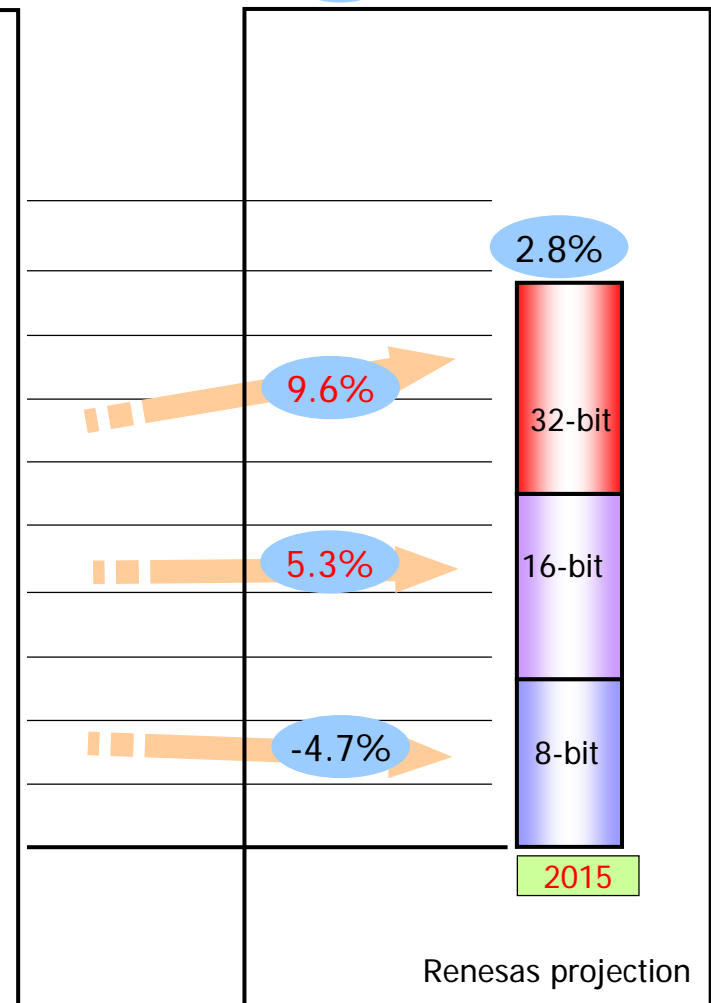
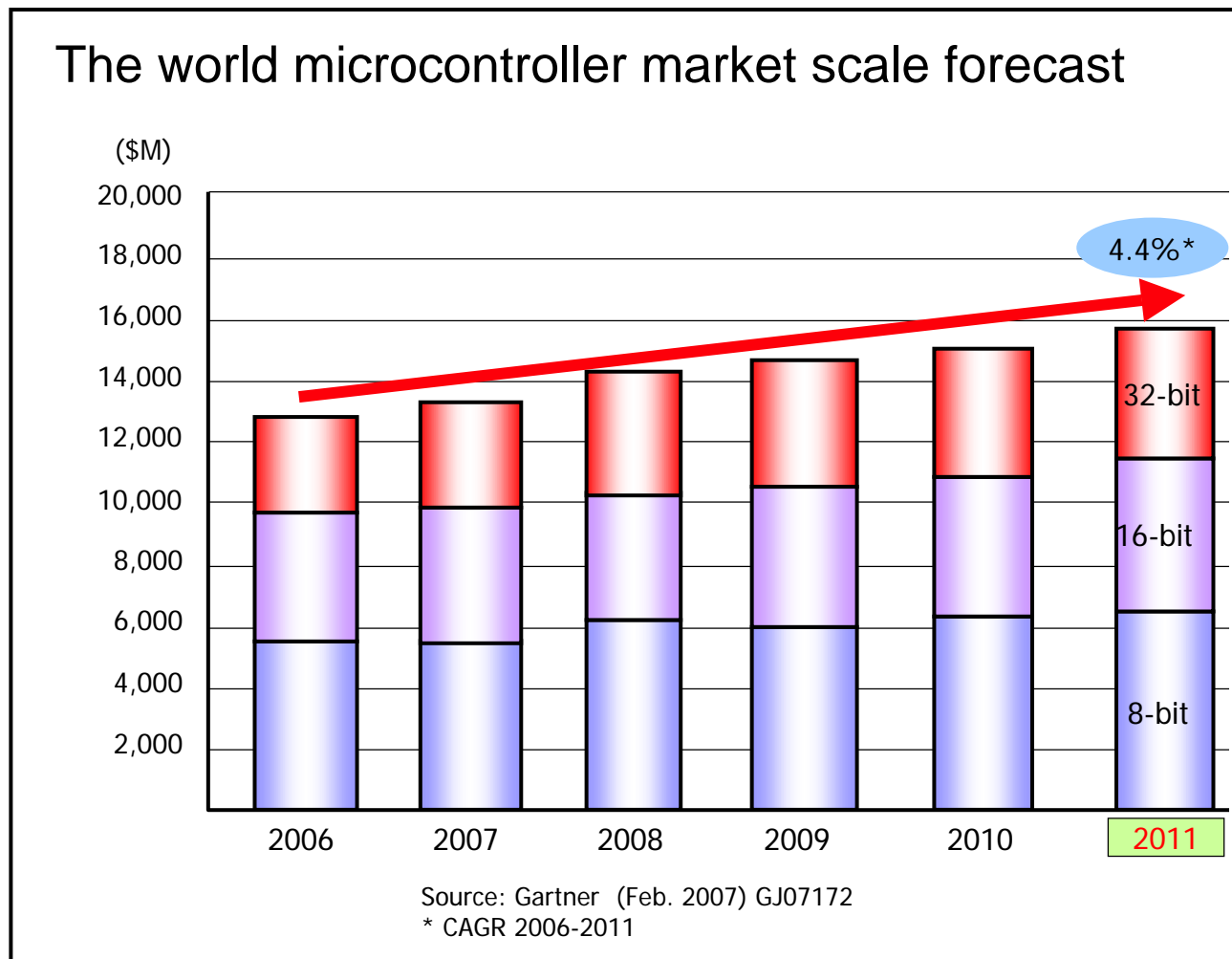
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WW Microcontroller Market Forecast



- 16-bit and 32-bit MCUs will become the mainstream for embedded applications.

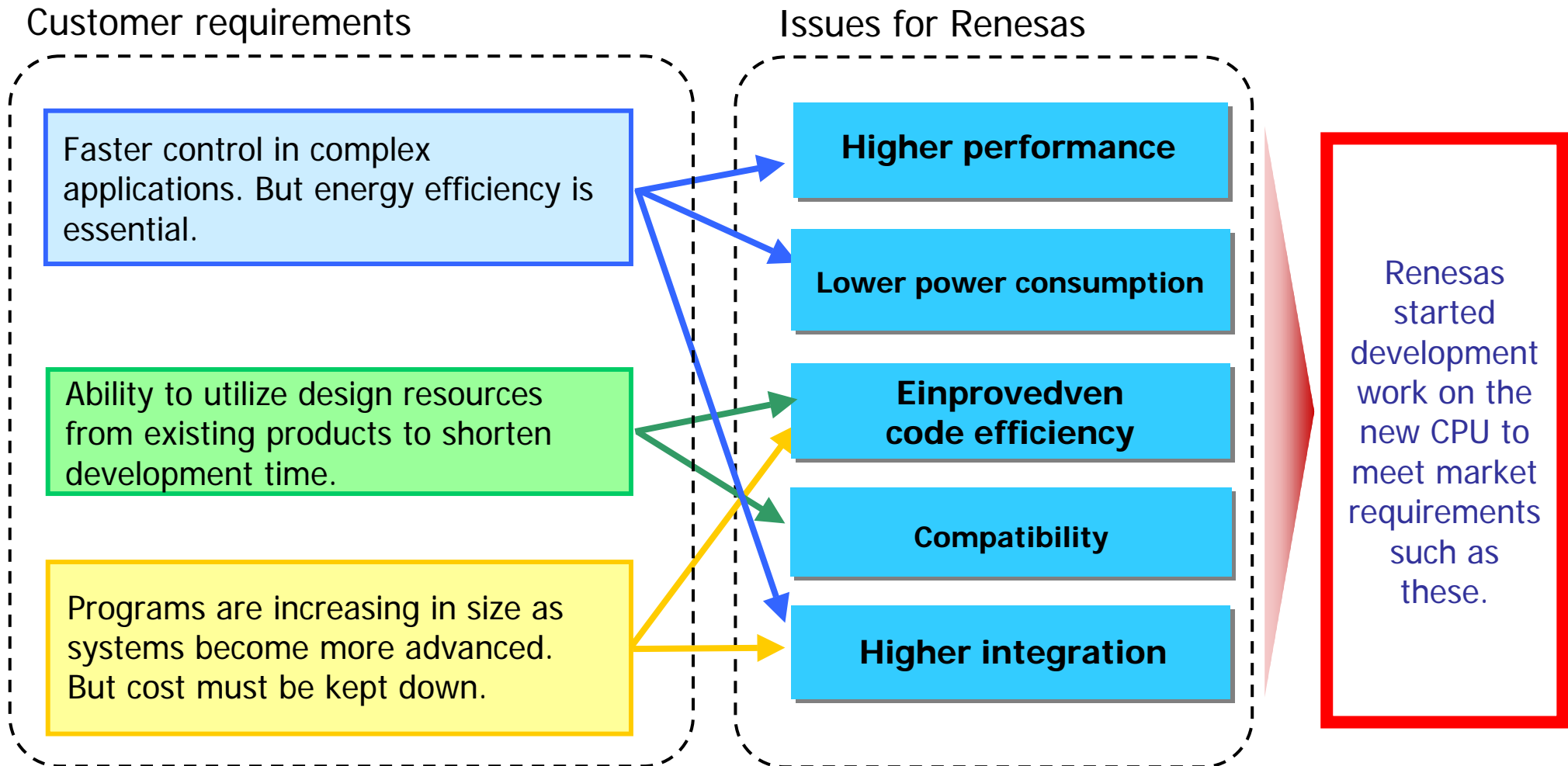
● : Average annual growth rate



Embedded Application Market Requirements



- Changes in embedded devices bring with them a variety of requirements.



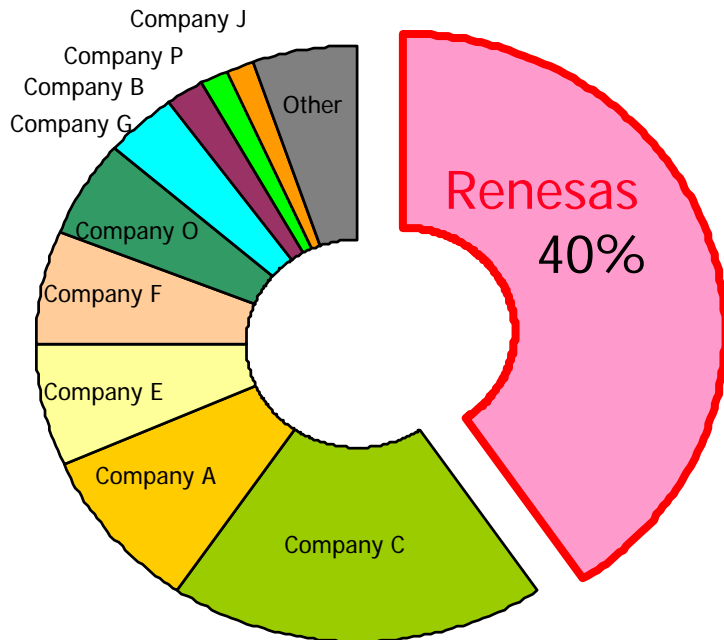
Positioning on Roadmap



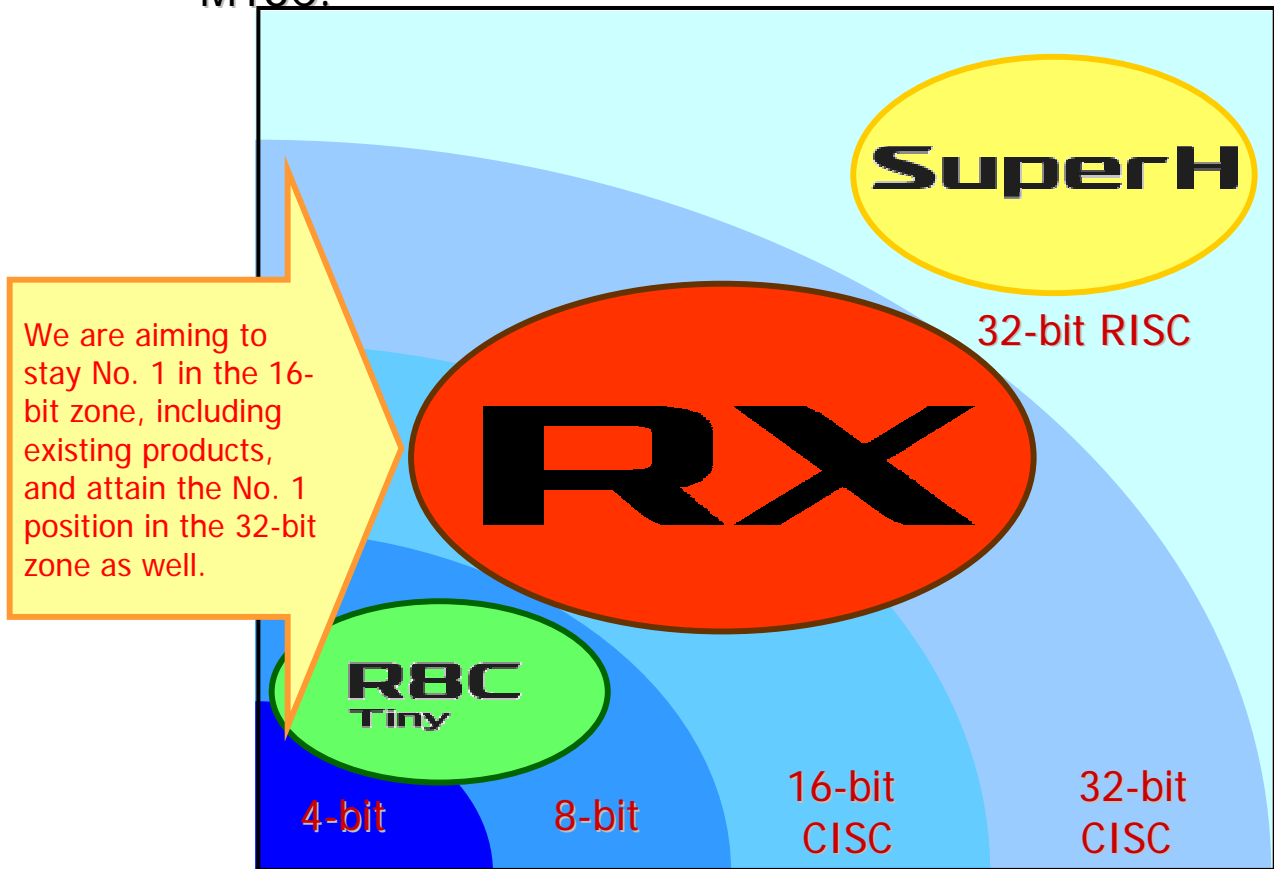
- Coinciding with the 5th anniversary of the establishment of Renesas, we began development work on a new CPU for the 16-and 32-bit zones.

The “**next-generation CPU**” now under development inherits the DNA of the H8 and M16C.

16-bit MCU market share
(CY2006, value basis)



Source: Renesas estimates



Family Name of New CPU



Next-generation CISC CPU

RX Family



RX=***Renesas e******Xtreme***

*Next-generation CISC CPU-based MCUs from Renesas
offering outstanding performance and flexibility.*

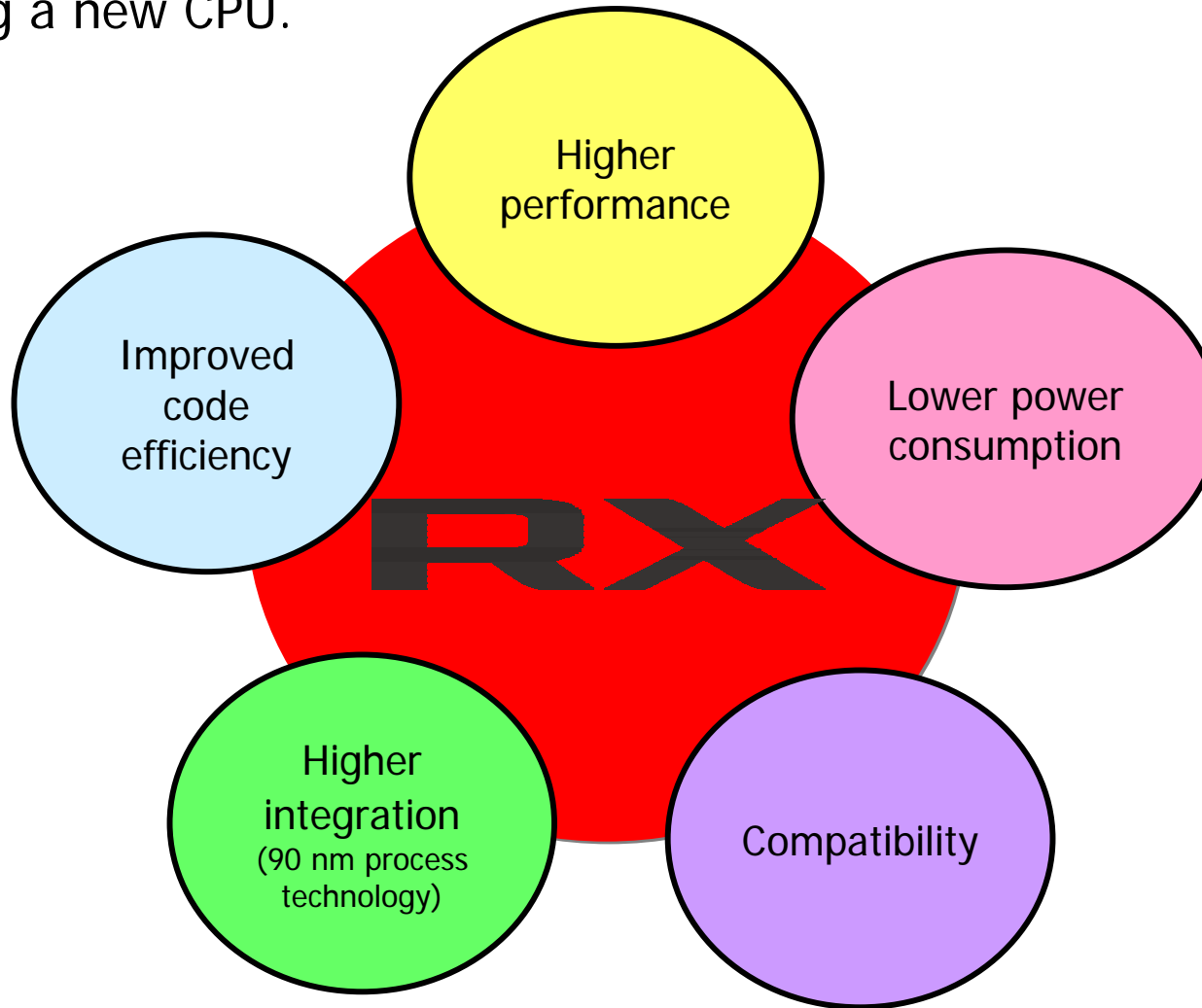
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Concept of RX



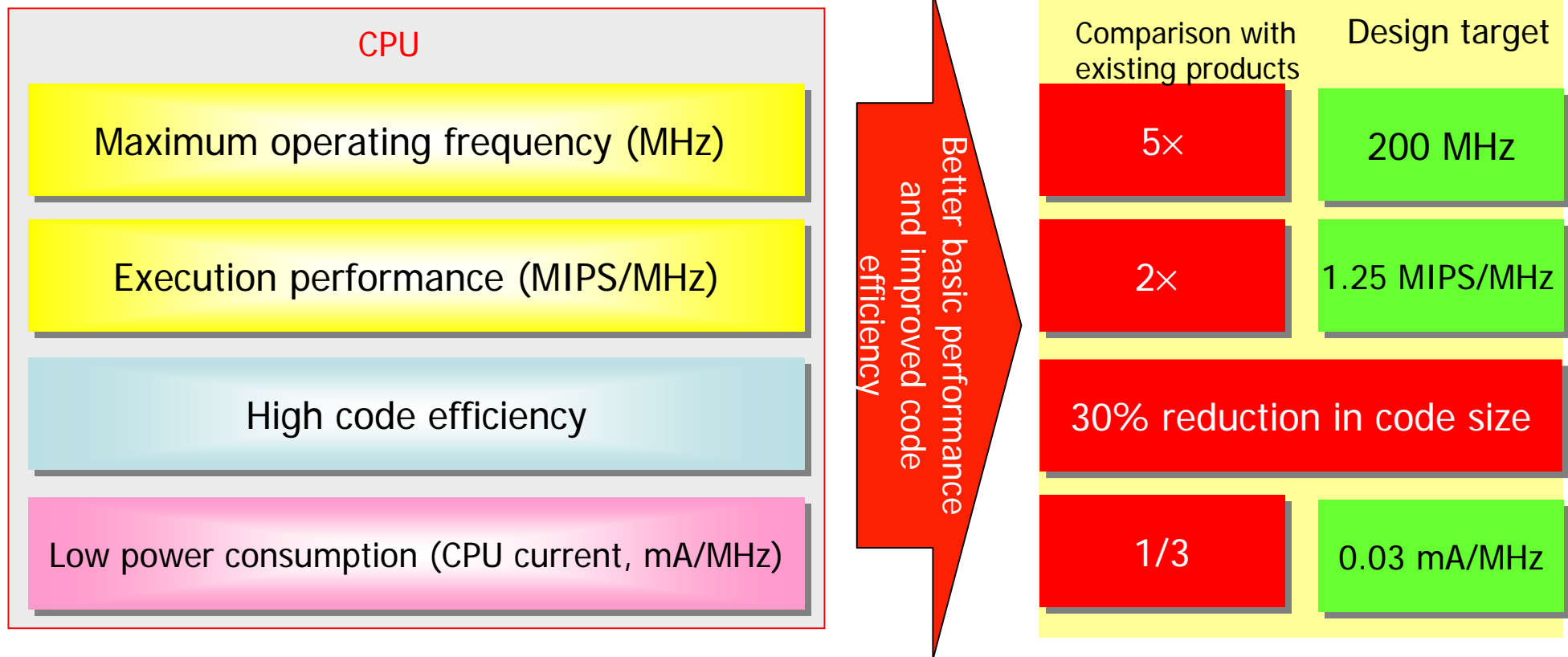
- We will overcome a variety of problems and meet the demands of the market by developing a new CPU.



Target Performance of RX



- The RX will be fabricated using a 90 nm process to achieve improvements in maximum operating frequency, performance, code efficiency, and reduced power consumption.



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RX CPU Features (1) – World-top-level performance –

- Operating frequency of 200 MHz, the highest level available in a CISC MCU
- 16 32-bit general registers
- ➡ A configuration using 16 32-bit general registers was found to provide optimal code efficiency and performance, based on a variety of benchmark tests.
- Execution in fewer clock cycles for basic instructions that are used frequently in current CPUs
- ➡ Faster execution of frequently used basic transfer and operation instructions.
- Floating-point instructions that support operations with general registers
- ➡ The on-chip single-precision floating-point unit delivers superior performance in control operations (digital filter operations, Fourier operations, vector operations, etc.) (and also supports add, subtract, compare, multiply, divide, and integer ↔ floating point convert instructions).

RX CPU Features (2) – World-top-level performance –



- Enhanced 32-bit multiplier, divider, and multiply-and-accumulate unit for high speed and excellent performance

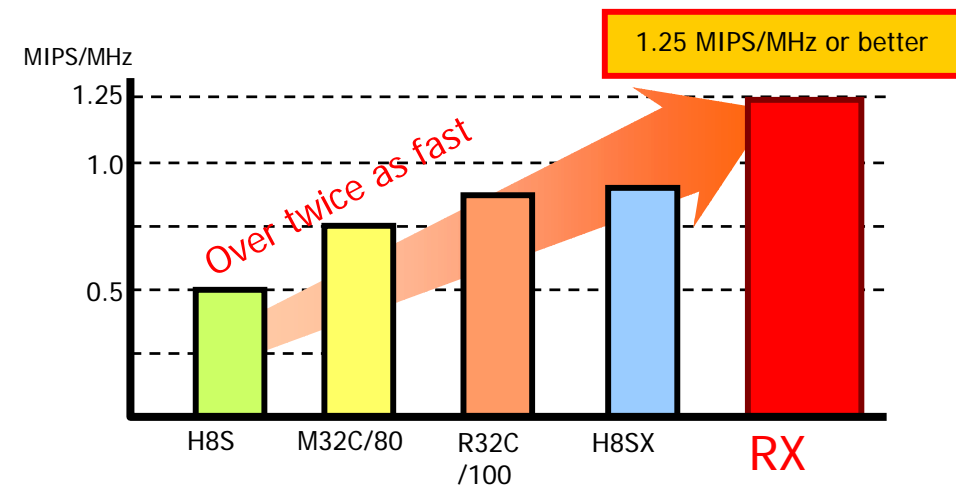
➡ Multiply instructions: $32\text{-bit} \times 32\text{-bit} = 64\text{-bit}$

➡ Divide instructions: $32\text{-bit} \div 32\text{-bit} = 64\text{-bit}$

➡ Multiply-and-accumulate instructions: $32\text{-bit} \times 32\text{-bit} + 80\text{-bit} = 80\text{-bit}$

- Harvard architecture for high-speed instruction fetches and data accesses

➡ Processing performance of 1.25 MIPS/MHz* or better



* When running Dhrystone 2.1

RX CPU Features (3) – World-top-level code efficiency –



- Variable-length instructions, with the length variable in byte (8-bit) units, for better code efficiency
- Assignment of frequently used instructions to short instruction codes for better code efficiency than existing CPUs

➡ Transfer, branch, compare, add, subtract, shift instructions, etc.

- Addition of new instruction formats and addressing modes

➡ 3-operant format (ADD, SUB, AND, OR, MULU, etc.)

(Previous) MOV Rs2,Rd
ADD Rs,Rd

➡ 1 fewer instruction

(RX)ADD Rs,Rs2,Rd

➡ Addition of addressing modes ideal for array and pointer operations (indexed register indirect, port-increment, pre-decrement, etc.)

(Previous) ADD #4,Rb
MOV Rs,[Rb]

➡ 1 fewer instruction

(RX)MOV.L Rs,[Ri,Rb]

- Register configuration consisting of 16 32-bit registers to facilitate compiler optimization

RX CPU Features (4) – World-top-level code efficiency –



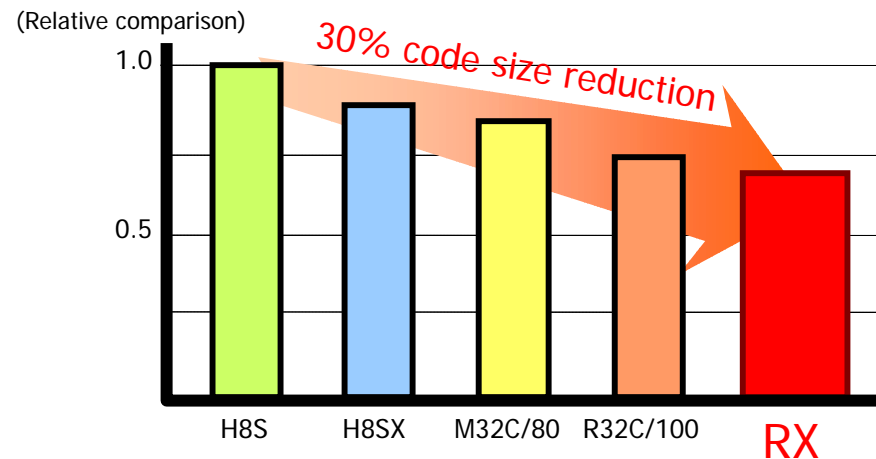
■ Better code efficiency than earlier CPUs through improved compiler optimization

➡ Reduced code size through active utilization of new functions and additional registers.

➡ Better code efficiency allows developers to select an MCU with less on-chip memory, helping to reduce overall system cost.



30%* code size reduction compared with earlier CPU



* When running Dhrystone 2.1

RX CPU Features (5)



– Lower power consumption, higher integration, compatibility/continuity –

Lower power consumption, higher integration

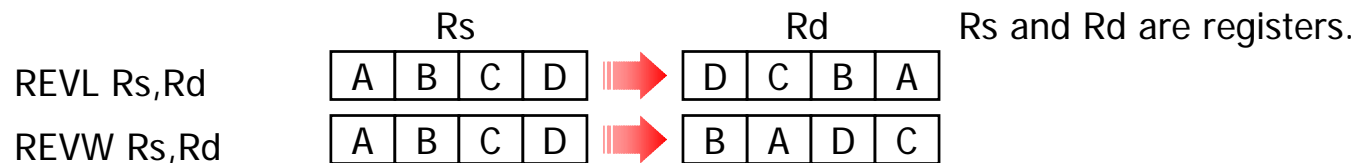
- Newly developed 90 nm low-leak, low-current process technology
- Optimized logic and circuit design



CPU power consumption as low as 0.03 mA/MHz or less

Compatibility/continuity

- Availability of optimized tools enabling utilization of software developed for earlier Renesas CPUs (M16C/R32C, H8S/H8SX)
- Support for bi-endian* data access
 - ➡ Data access continuity with earlier products
(The M16C is little-endian and the H8S is big-endian.)
- Support for endian format conversion instructions to assure compatibility with data formats of existing CPUs



* Selectable between big-endian and little-endian



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Summary

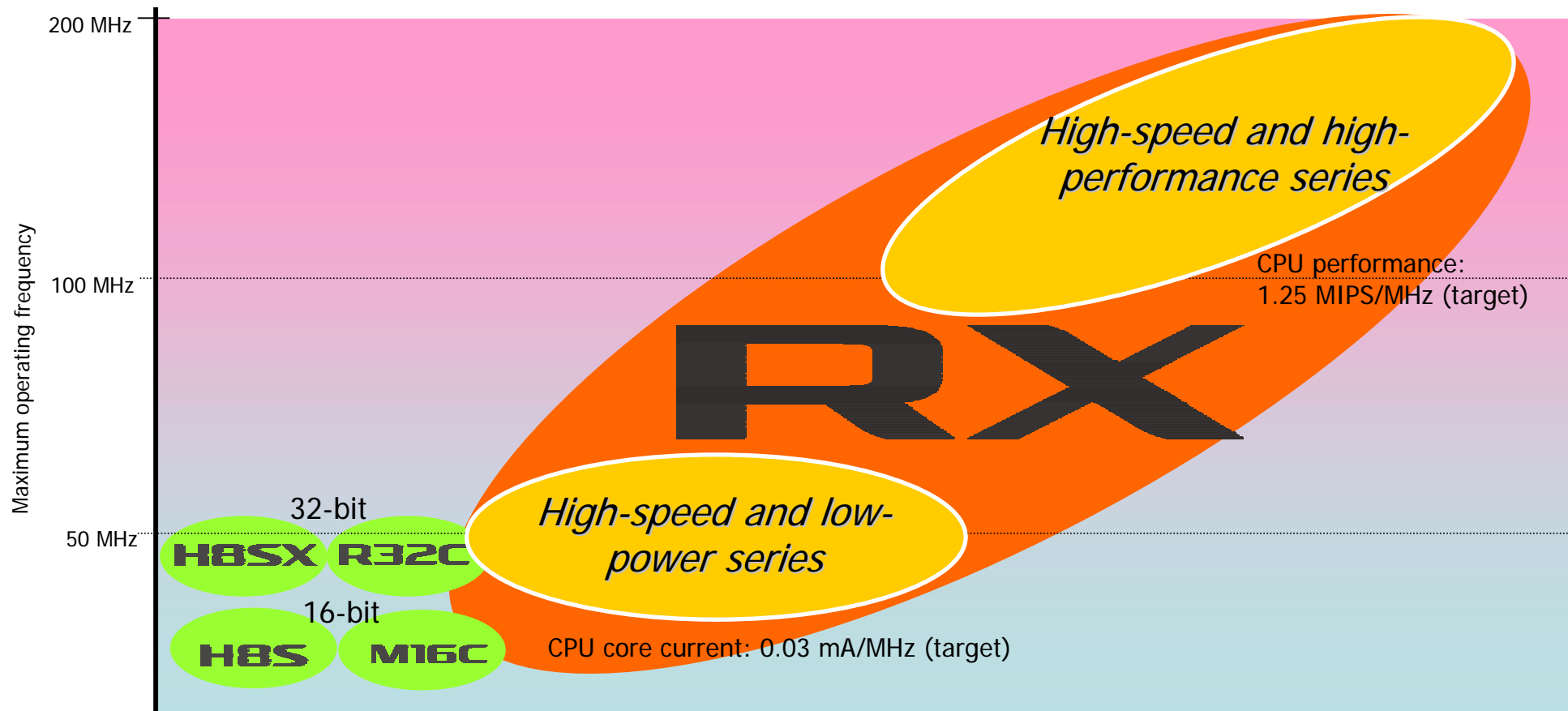
- The new CPU will be named the RX.
- The RX will deliver world-top-level performance and code efficiency.
- The RX realizes low power consumption and continuity.
- The RX CPU core will be general-purpose and suitable for a wide range of embedded applications.

RX Family Development Plans



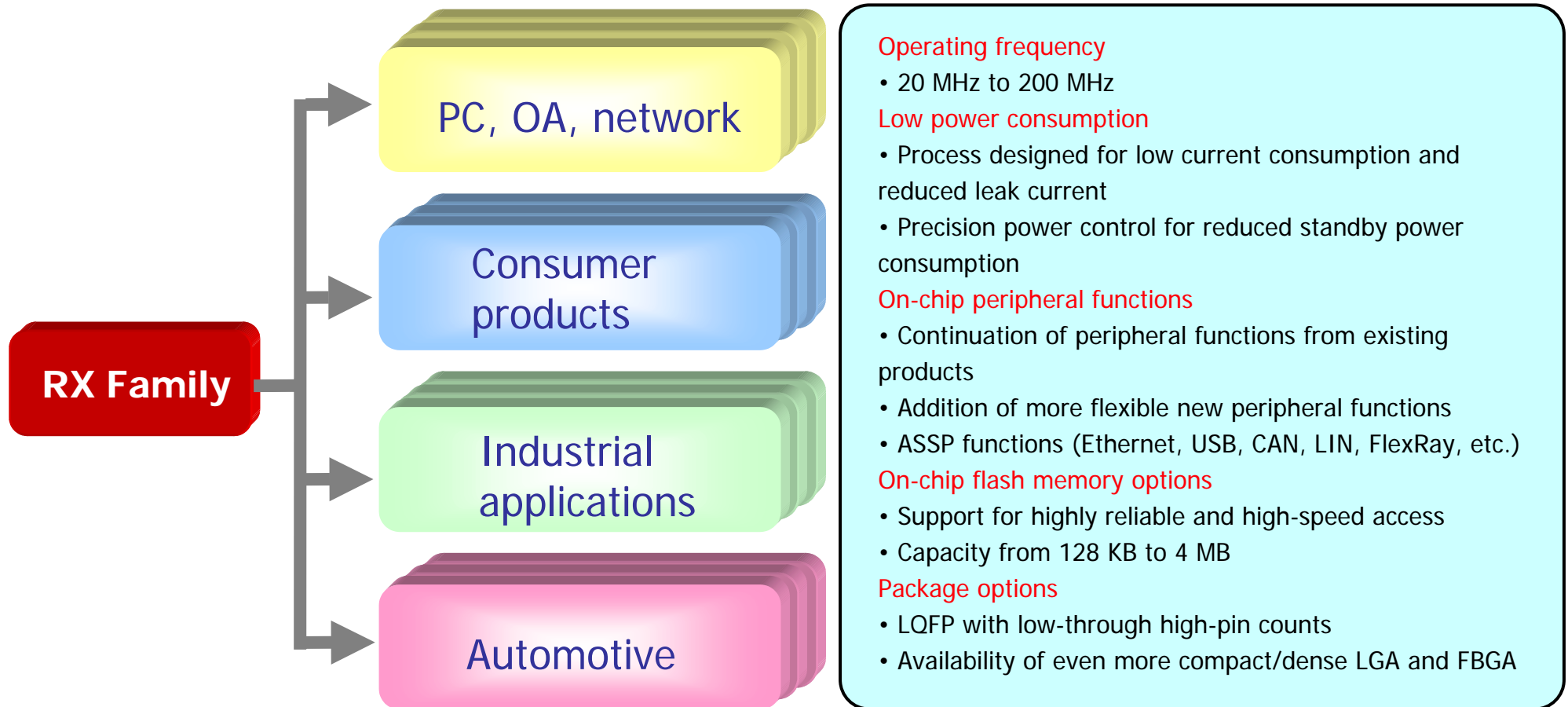
The RX Family will be developed into two series of products, one focusing on high speed and high performance and the other focusing on high speed and low power consumption.

The first products in the RX Family for office equipment, digital consumer products, and industrial applications will have an operating frequency of 100 MHz and are scheduled for release in the second quarter of FY2009.



RX Family Rollout Plans

- We will offer a range of products with strong competitiveness in many different fields.





Renesas Technology Corp.

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The Renesas logo features a stylized red 'R' icon on the left, followed by the word 'RENESAS' in a bold, red, sans-serif font. The 'R' icon is composed of a square base and a curved top that tapers to a point.

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