

Introduction of the New Renesas CPU Architecture

Renesas Technology Corp.
MCU Business Group

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1. New CPU and MCU Roadmap

1-1. Positioning on Roadmap

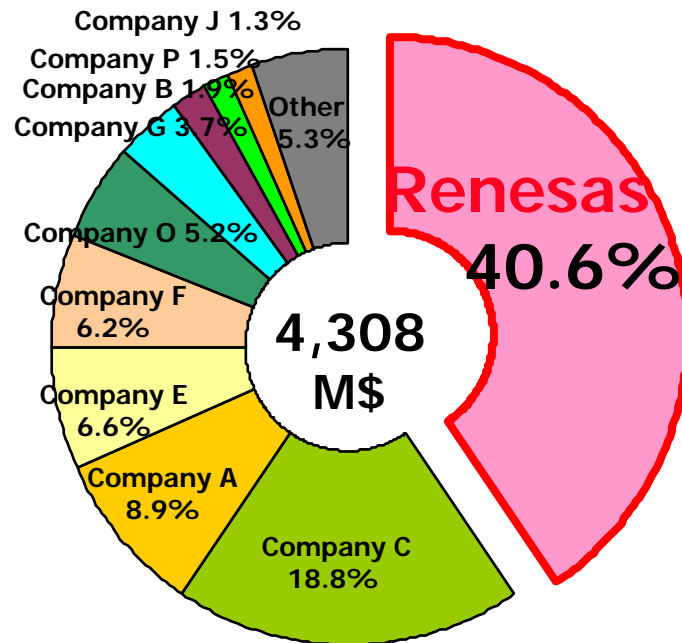
1-2. New CPU Development Concept

Positioning on Roadmap

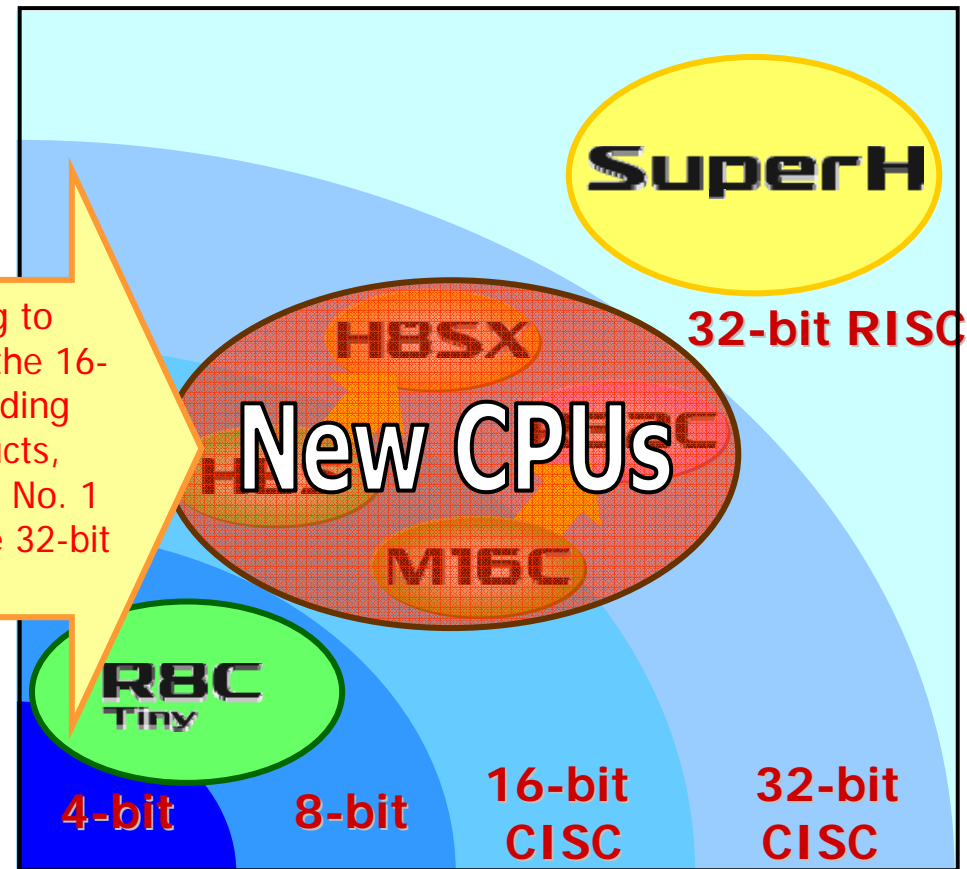
■ Coinciding with the 5th anniversary of the establishment of Renesas, we have begun development work on new CPUs for the 16- and 32-bit zones.

The **“next-generation control CPUs”** now under development will inherit the DNA of the H8 and M16C.

16-bit MCU market share
(CY2006, value basis)



We are aiming to stay No. 1 in the 16-bit zone, including existing products, and attain the No. 1 position in the 32-bit zone as well.



Source: Gartner Dataquest (March 2007) GJ07220

New CPU Development Concept

■ Development history of Renesas MCUs

2008: New CPUs

- More advanced architecture and improved performance
- Larger memory capacity and increased speed (up to 4 MB, up to 200 MHz)

2000s: R32C, H8SX

- 32-bit architecture
- Large memory capacity and high speed (up to 1 MB, up to 100 MHz)

1990s: M16C, M32C, H8S

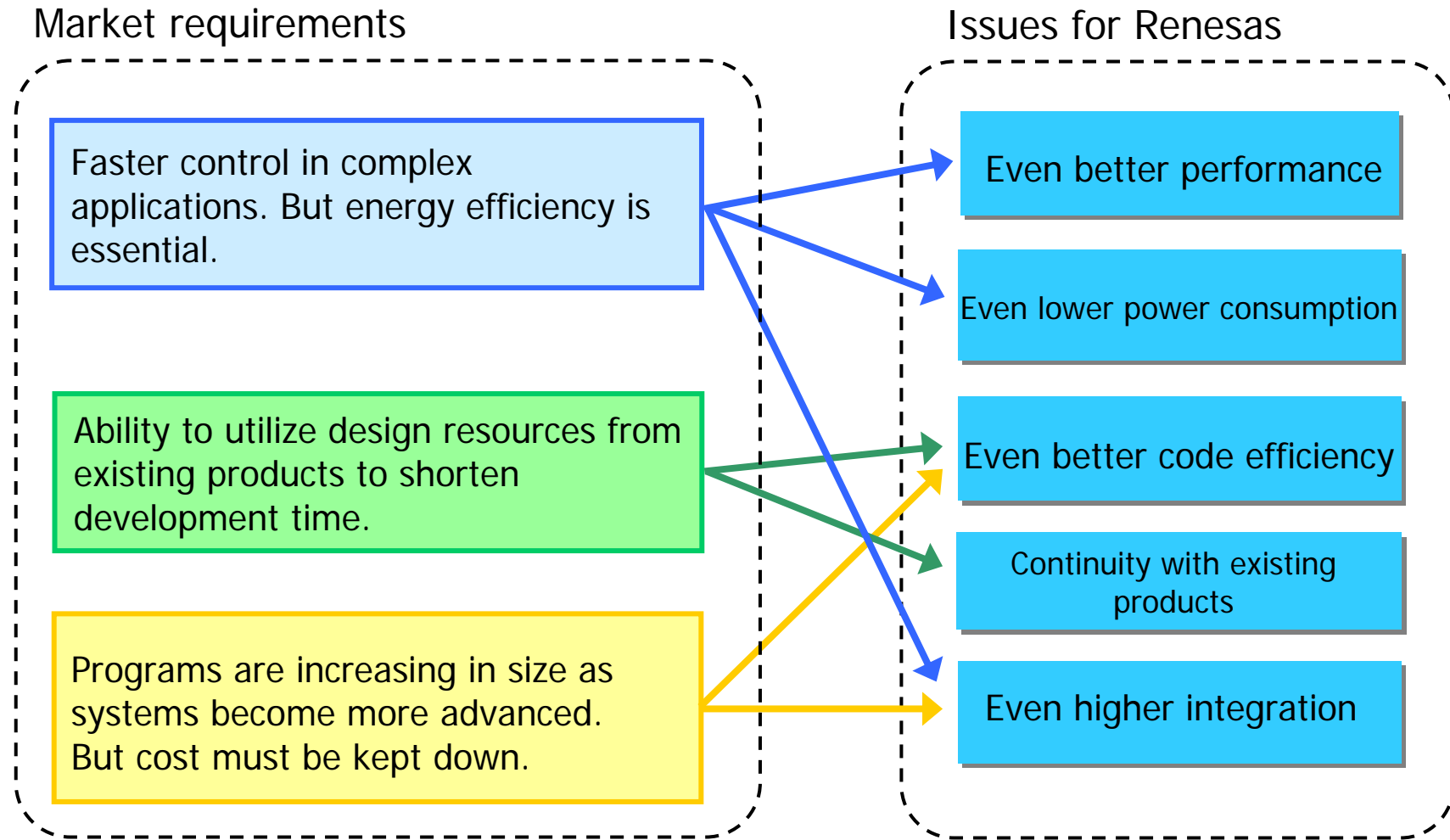
- Larger flash memory capacity (up to 512 KB)
- Improved performance, higher operating frequency (up to 40 MHz)

1980s: 7700, H8

- Proprietary 16-bit architecture
- Start of development work on flash MCUs

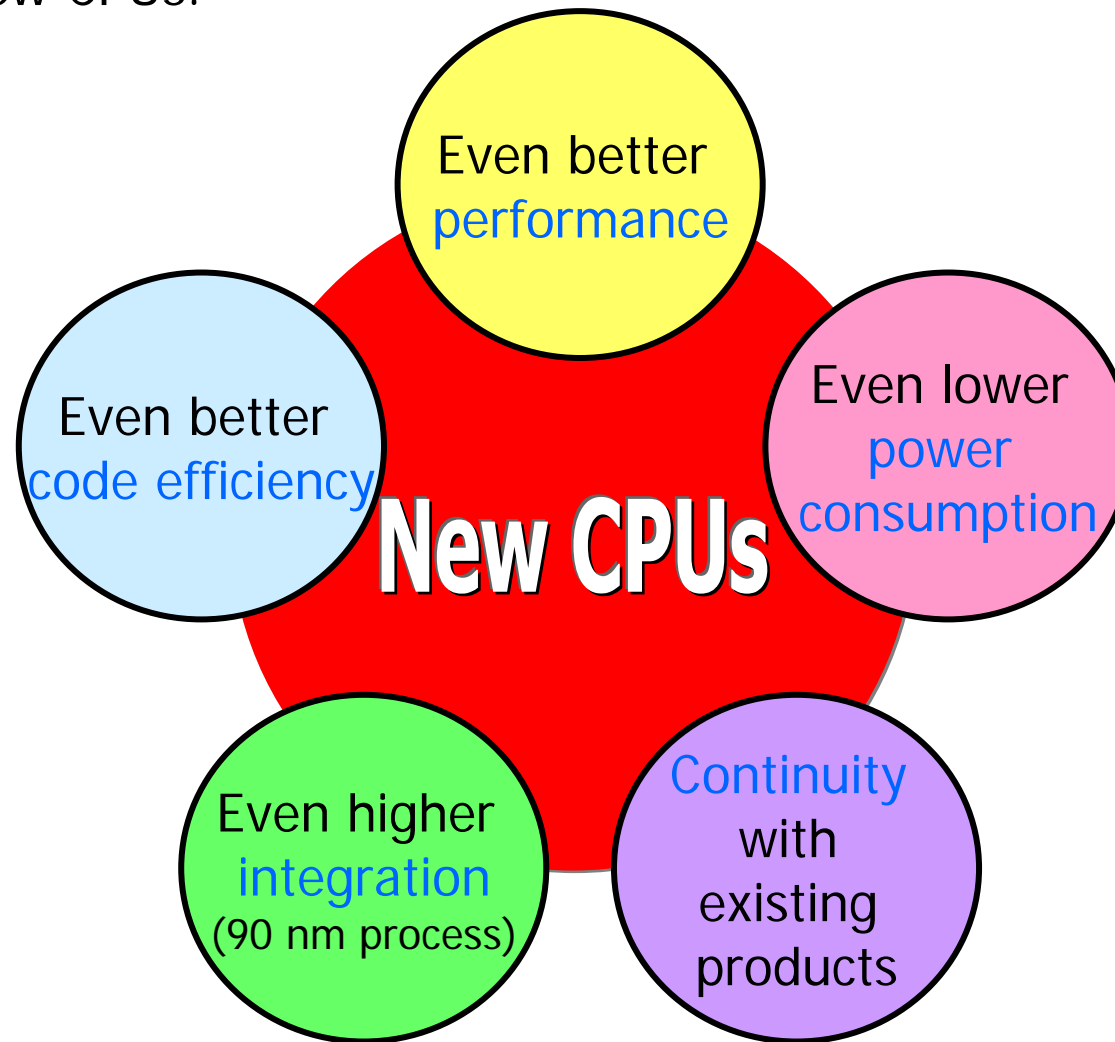
Embedded Application Market Requirements

- Changes in embedded devices bring with them a variety of requirements.



New CPU Concept

■ We will overcome a variety of problems and meet the market needs by developing new CPUs.



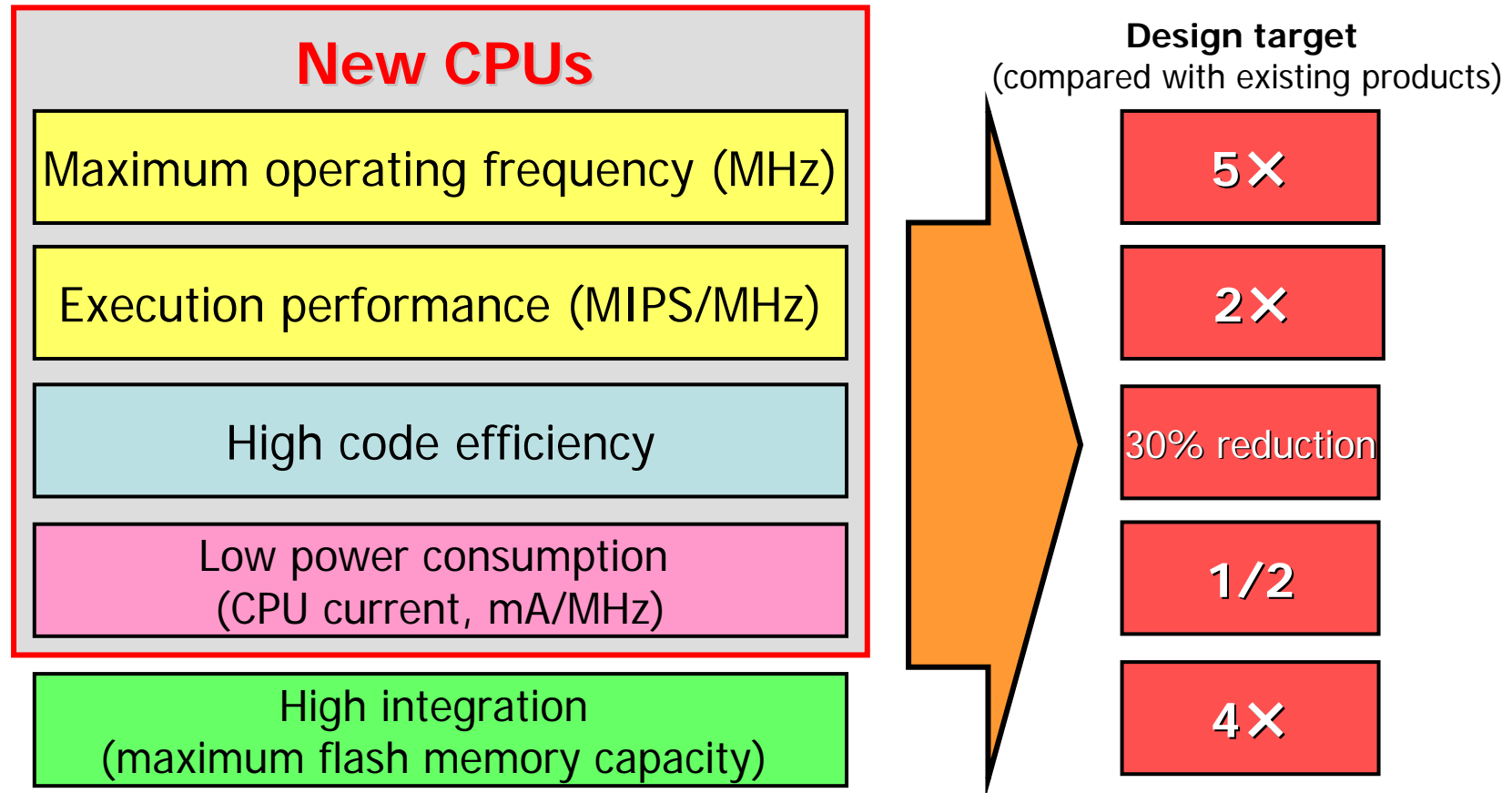
2. Object of New CPU Rollout

2-1. Target Performance of New CPUs

2-2. Emphasis on Compatibility with Existing MCUs

Target Performance of New CPUs

■ Substantial improvements in performance, code efficiency, reduced power consumption, and integration.



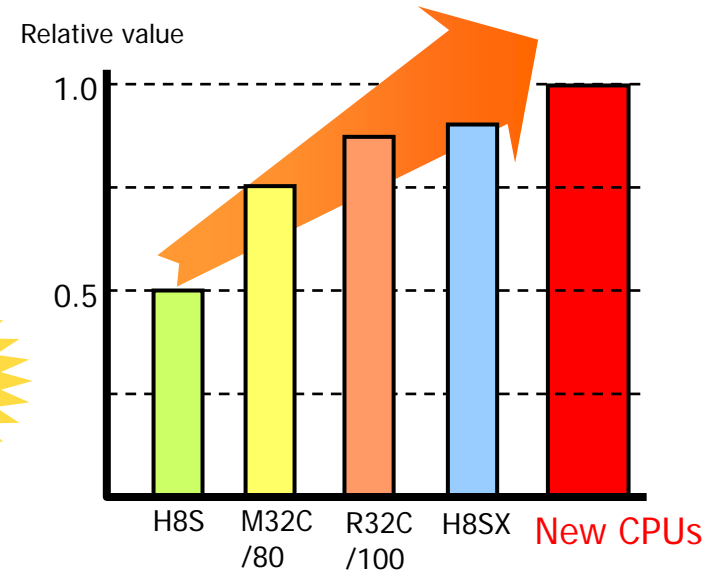
Even Better Performance

We aim to achieve 10 times (twice the processing performance times five times the operating frequency) the performance by boosting processing performance and operating frequency.

Improved processing performance (MIPS/MHz)

- Reduced memory access by **increasing the number of general registers**
- **New combined instructions** for faster execution speed
- **High-speed on-chip flash memory** using 90 nm process

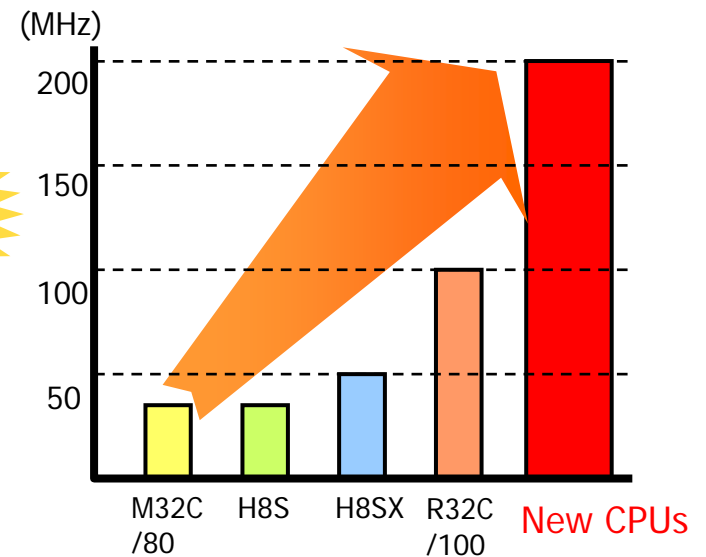
Twice the processing performance



Higher maximum operating frequency

- **Reexamination of architecture** and optimized design
- **Ultrafine 90 nm process** for higher speed

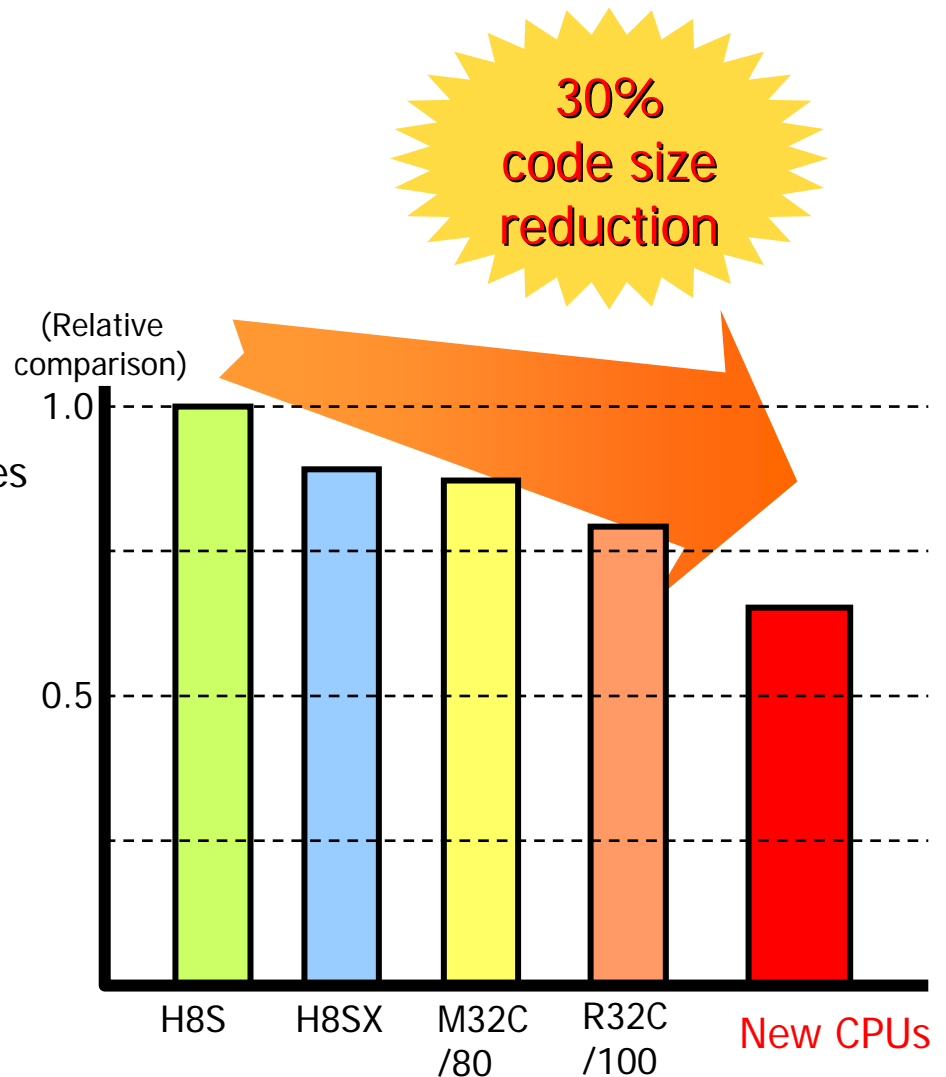
Max. operating frequency: 5x



Even Better Code Efficiency

We aim to reduce code size by about 30%.

- Enhanced architecture designed to exploit the advantages of **variable-length instructions (byte units)**
 - **Shorter code length** for high-frequency instructions and high-frequency addressing modes
 - Addition of **new combined instructions** suitable for embedded applications
- Better optimization using **compiler**

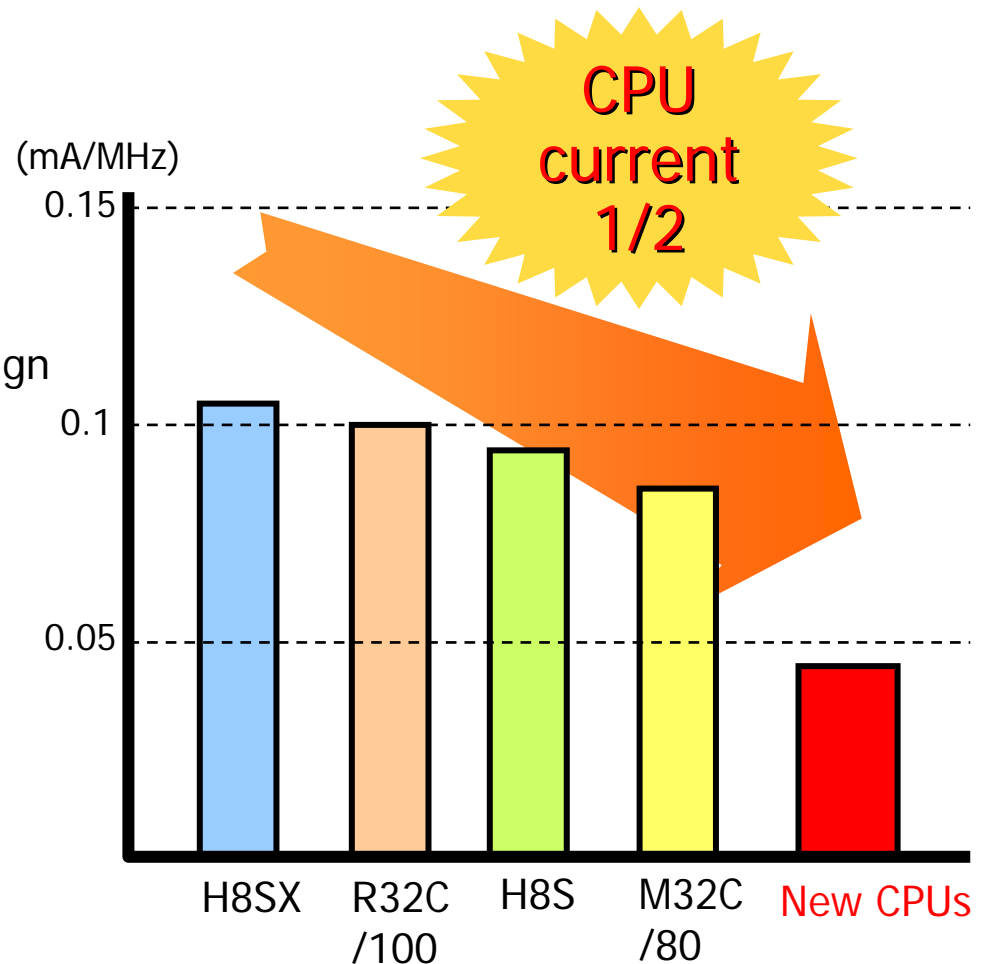


Note: Relative values based on Renesas program code

Even Lower Power Consumption

We aim to reduce CPU current consumption by half.

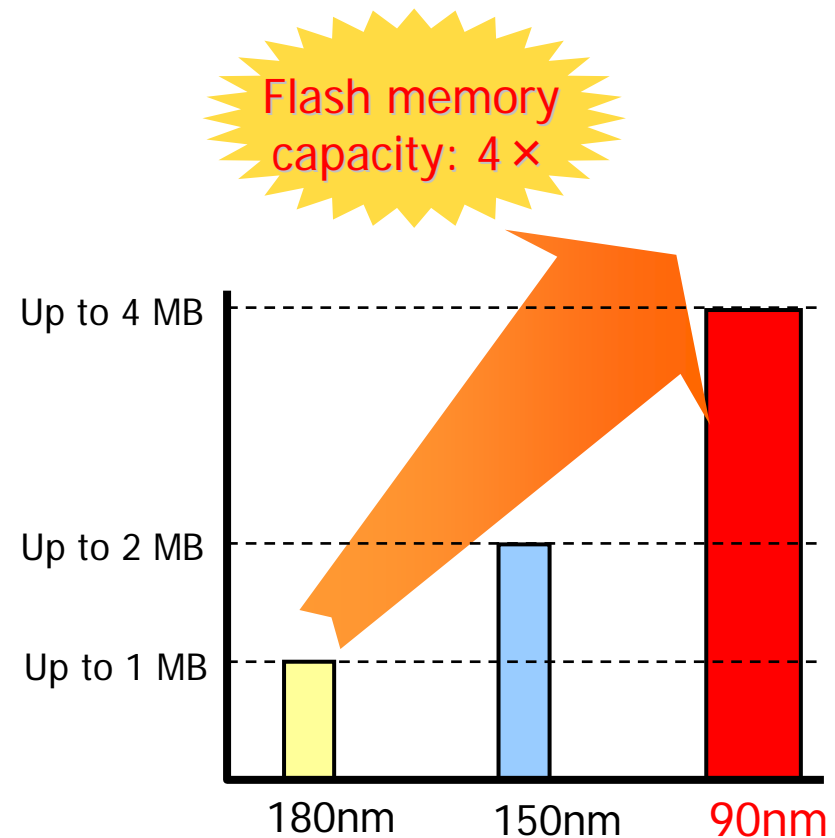
- Reduced current consumption during normal operation
 - Reexamination of architecture to reduce number of gates
 - Clock gating technology and optimized design
- Reduced current consumption in low-power mode
 - Process designed for lower leak current
 - Highly precise power control



Higher Integration/More Advanced Flash Memory

We are using a leading-edge 90 nm process to create a product lineup combining large-capacity flash memory and a full array of peripheral functions.

90 nm flash MCU
<Product with 2.5 Mbytes of on-chip flash memory>



Emphasis on Compatibility with Existing MCUs

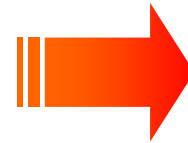
■ We will emphasize compatibility with the M16C and H8S Families while aiming for **“the world’s best low-power operation and code efficiency.”**

Even better

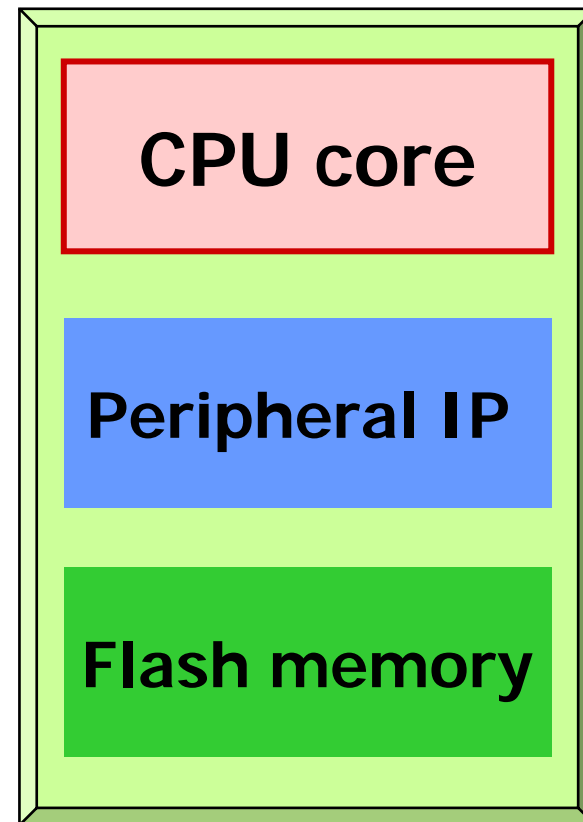
Architecture emphasizing continuation of the strong points of the M16C and H8S families

Continuation of peripheral IP from M16C and H8S families with further performance improvements

High speed and large capacity (90 nm process)

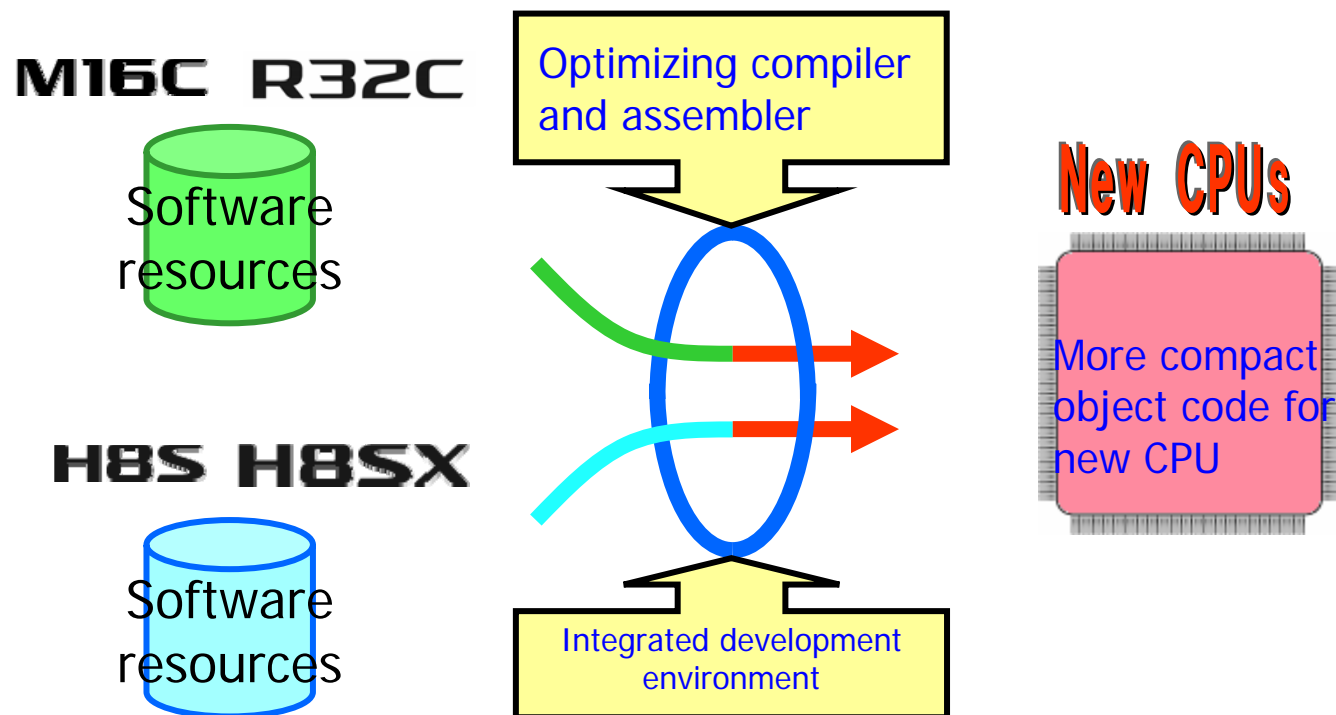


Products with new CPUs



Software consistency

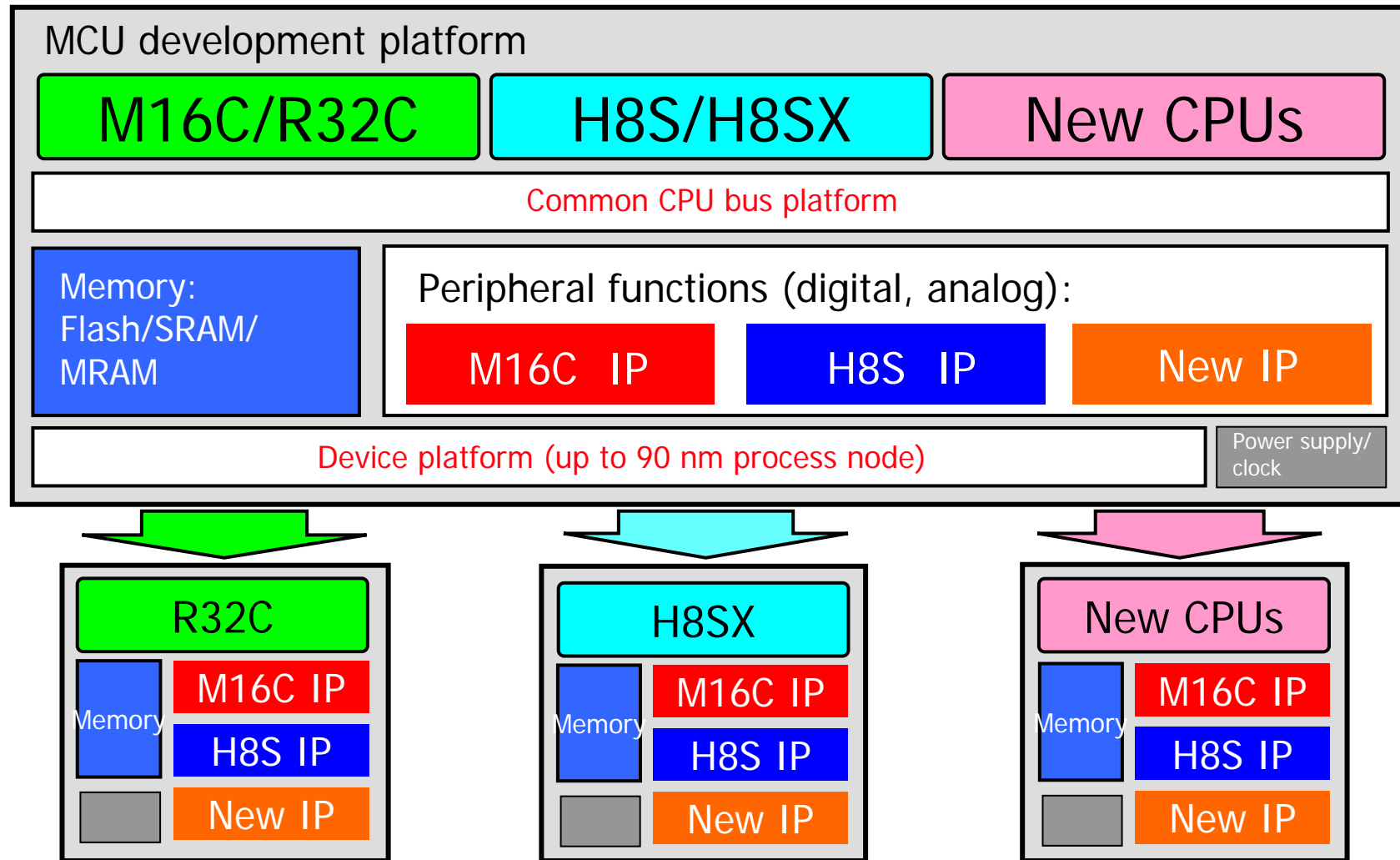
1. Ability to reuse existing C source code
2. Ability to reuse existing assembler code for the M16C Family and H8 Family
3. Continuation of existing OS API



API: Application Program Interface

Continuation of Peripheral Functions

We will build a common MCU development platform with existing products and strengthen our product lineup. The new CPUs will inherit the peripheral functions of existing products.

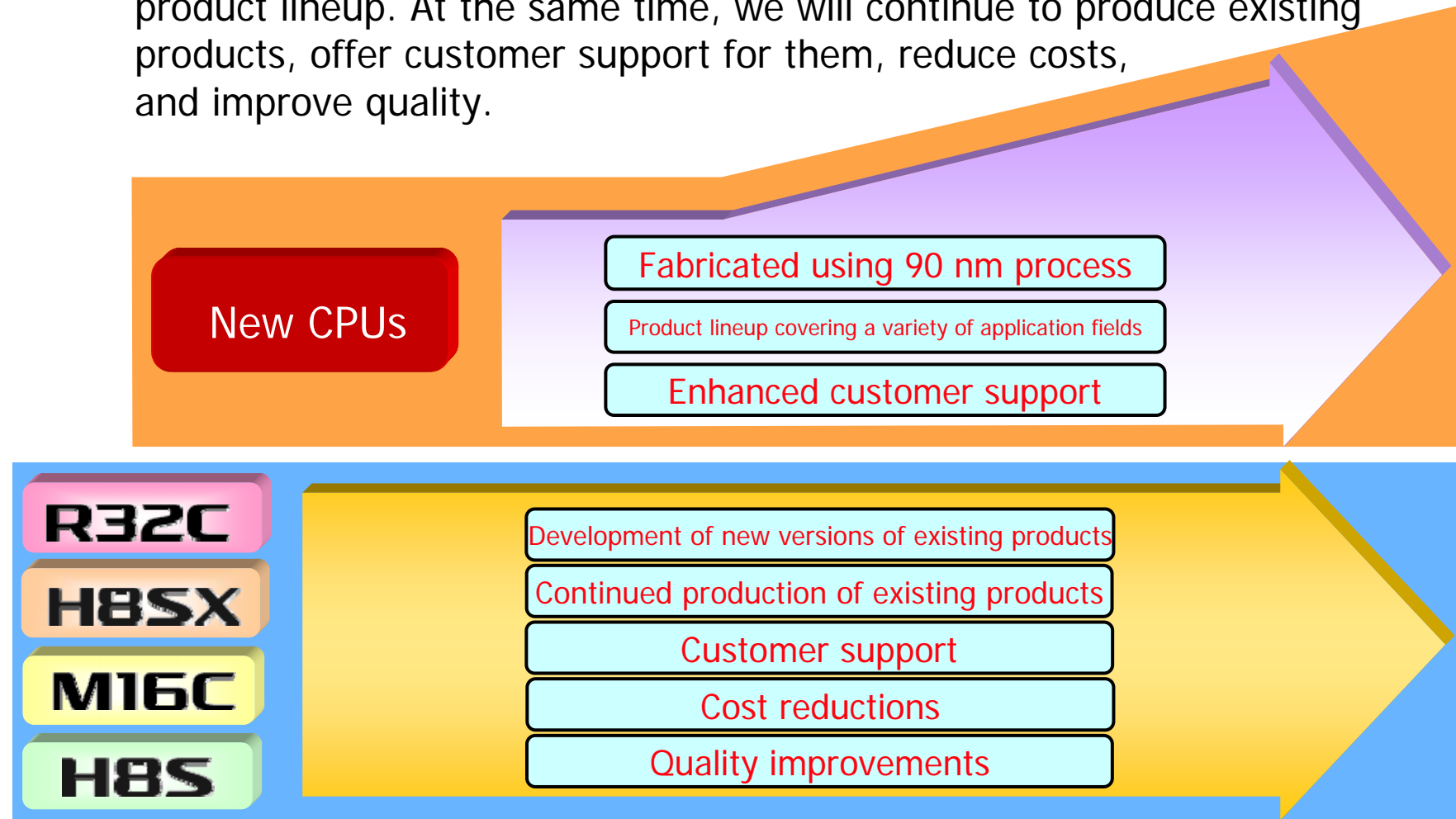


3. New CPU Rollout Policy

- 3-1. Product Development, Production, and Customer Support Policies**
- 3-2. New CPU Rollout Plans**
- 3-3. New CPU Development Environments**

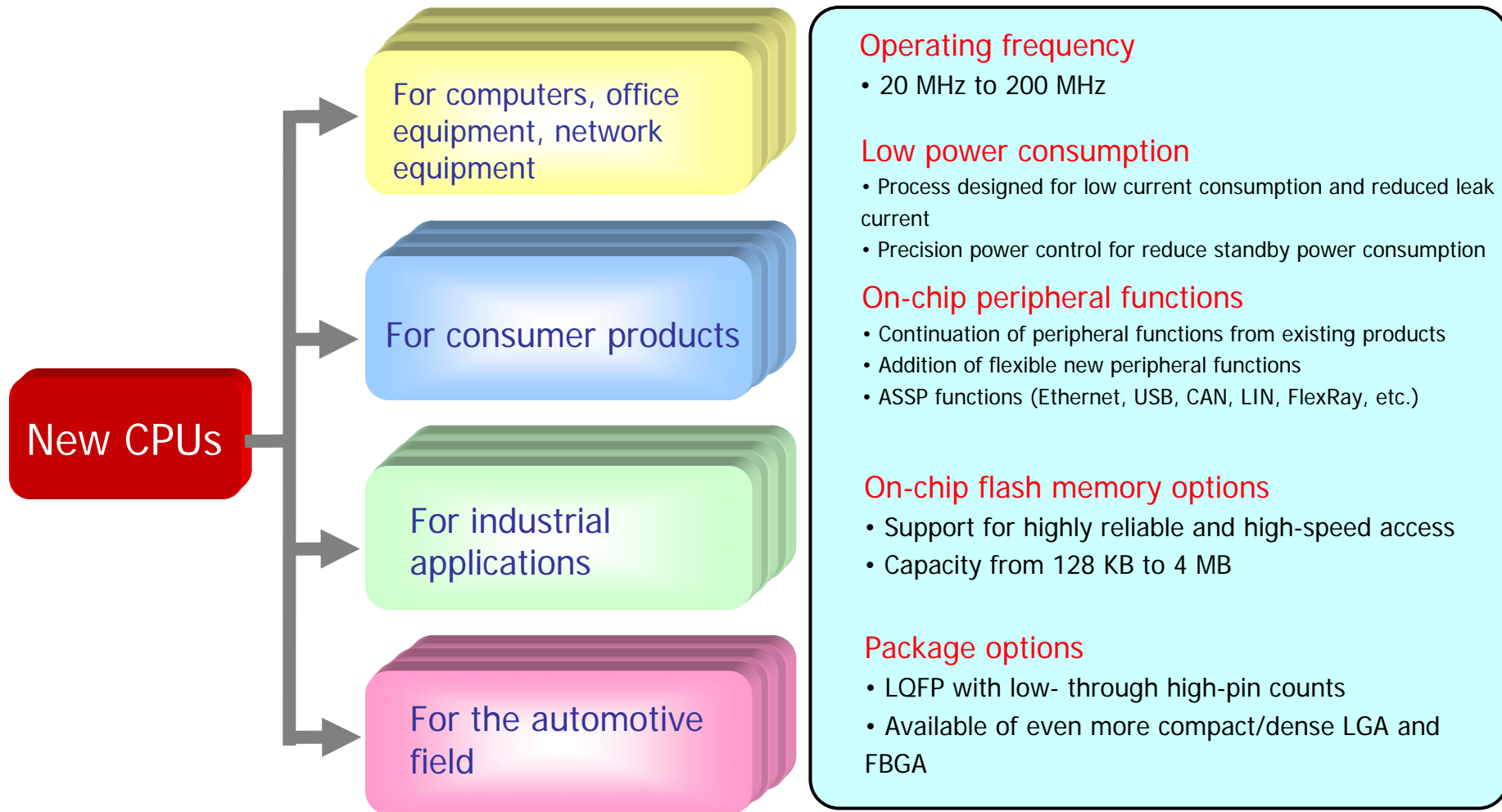
Product Development, Production, and Customer Support Policies

- New CPUs: We will use a 90 nm process, develop new products, and provide enhanced customer support.
- Existing CPUs: We will continue to develop new products and strengthen our product lineup. At the same time, we will continue to produce existing products, offer customer support for them, reduce costs, and improve quality.



New CPU Rollout Plans

■ We will offer a range of products with strong competitiveness in many different fields.

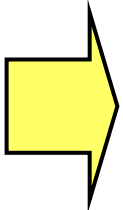
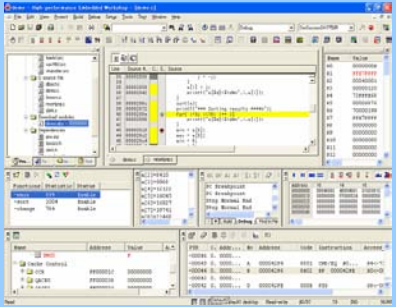


LIN (Local Interconnect Network) is a specification for building affordably priced networks. The LIN standard was established by the LIN Consortium.

New CPU Development Environments


Products based on the new CPUs will support development environments equivalent to those for existing products to ensure maximum convenience for customers.

Integrated development environment (HEW)

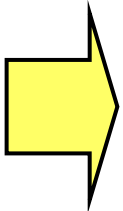


Supports convenient program development in the same manner as with existing products.

Full-spec emulators

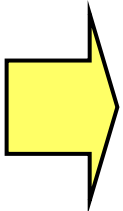


On-chip emulators



A variety of emulators are available to match the scale of development.

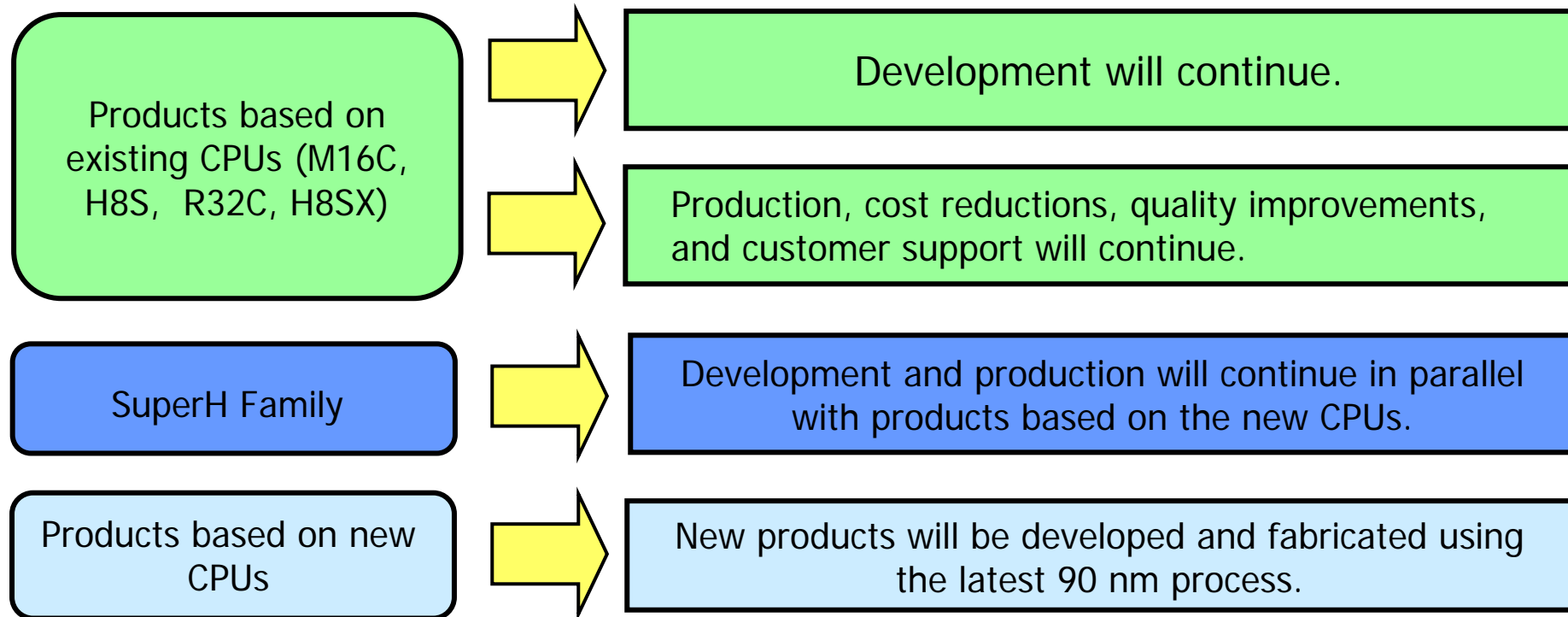
Starter kits (RSK)



A development environment package including a CPU board ideal for learning about MCUs.

HEW: High-Performance Embedded Workshop

Conclusion





Renesas Technology Corp.

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