

Renesas Technology Releases SuperH™ Family SH7652 Offering Industry-First Support for Both IP Broadcasting and DTCP-IP Copyright Protection

— On-chip Ethernet controller, enabling simultaneous 2-channel network transmission of HD (High Definition) digital content —

Tokyo, November 15, 2006 — Renesas Technology Corp. today announced the 32-bit SuperH*¹ Family SH7652 microprocessor with an on-chip Ethernet controller, incorporating the industry's first encryption/decryption functions supporting both the copyright protection function for IP broadcasting*² will start in Japan, and the DTCP-IP*³ copyright protection standard for in-home distribution, for use in digital audiovisual and office automation devices with built-in network functions. Sample shipments will begin in January 2007 in Japan.

As enhancements to current 133 MHz SH7650 with DTCP-IP functions, the SH7652 features the addition of a copyright protection function for IP broadcasting in Japan, a more comprehensive range of peripheral functions, and a 50% increase in operating speed to 200 MHz.

The SH7652 offers the following features.

- (1) IP broadcasting copyright protection, DTCP-IP for in-home distribution, and other copyright protection support functions plus Ethernet connection functions in a single-chip, enabling secure network transmission of HD digital content

The SH7652 includes an error correction function and encryption/decryption circuitry for decrypting IP broadcasting content, as well as functions compliant with the DTCP-IP standard used for content distribution within the home. These copyright protection authentication functions and content encryption/decryption functions are implemented using firmware to be provided together with the SH7652. These functions enable copyright protection processing and network processing to be handled by a single chip without further the host CPU burden. Moreover WM DRM10*⁴ copyright protection is also supported.

- (2) High-speed Ethernet controller, enabling simultaneous 2-channel transmission of HD digital content

An IEEE802.3 standard*⁵ compliant media access controller (MAC)*⁶ is incorporated, enabling connection to a 10/100 Mbps (megabit per second) Ethernet LAN. The improved processing performance makes it possible to perform IP broadcasting copyright protection processing and DTCP-IP control, and carry out simultaneous 2-channel transmission of HD digital content.

- (3) Comprehensive interface functions, including USB, SD Memory Card*⁷, and serial sound interfaces

A USB 2.0 High Speed compliant USB Host/Function module and SD Memory Card host interface are included, enabling connection to a memory card and wireless LAN module. Serial sound interfaces are also incorporated, allowing playback of MP3, WMA (Windows Media[®] Audio), and similar audio data well within the capacity of the high-performance CPU.

The SH7652 can easily be connected to another microprocessors or CPU via an on-chip host interface function. This function enables a main microprocessors performing system control to handle the SH7652 as an SRAM-equivalent device in performing data transmission and reception. This allows control as an Ethernet controller, enabling network related function development to be carried out independently, and simplifying user product development.

< Development Background >

Progress has been made in connecting digital home appliances compliant with DLNA*⁸ standard to a home network. Moreover, the inauguration of a digital broadcasting service dubbed IP broadcasting is planned in Japan, and the start of digital content distribution inside and outside the home will begin.

Meanwhile, authentication and content encryption processing between devices are essential when transferring copyright protected digital content via a network in order to protect content on the network from unauthorized access.

Renesas Technology previously released SH7650 featuring DTCP-IP content protection standard for in-home distribution compatible functions and an Ethernet controller, and has now developed the 32-bit SuperH Family SH7652 incorporating IP broadcasting copyright protection support functions, DTCP-IP in-home content protection standard compliant functions, and an Ethernet controller for the market growth.

< Product Details >

The SH7652 incorporates 32-bit SH-2A CPU core with a built-in double-precision FPU, and an Ethernet controller. With processing power of 480 MIPS (million instructions per second) at a maximum operating frequency of 200 MHz, and copyright protection support functions, it is ideal for use in digital audiovisual and office automation devices with built-in network functions.

The copyright protection support functions provided in the SH7652 comprise a hardware encryption/decryption circuit block, and firmware for encryption/decryption circuit block and content data transfer control.

The SH7652 includes two video stream port channels that enable high-speed transfer of MPEG-2*⁹ TS (Transport Stream) and MPEG-2 PS (Program Stream) format data. These ports can be connected to an MPEG-2 encoder/decoder chip, enabling encrypted data received via a network to be decrypted, and transferred to an MPEG-2 chip at high speed as MPEG-2 TS format video data. Also, performing high-speed encryption of content data by means of the on-chip encryption circuit before transmission via a network makes it possible to achieve simultaneous secure network transfer of HD digital content on two channels.

The SH7652 also includes a comprehensive range of peripheral functions.

A single-channel Ethernet controller is provided that facilitates connection to a 10/100 Mbps Ethernet LAN. This Ethernet controller incorporates an IEEE802.3 compliant MAC layer, and an accelerator that performs TCP/IP checksum computations automatically without software intervention, reducing the load on the CPU.

USB and SD Memory Card host interfaces are also included, allowing connection to external devices such as an external storage and a wireless LAN module. An on-chip serial sound interface and I²C bus used by digital audiovisual and office automation devices simplify system design, while the provision of a host interface function allows easy connection to a main microprocessor for user product control or the like. This interface performs high-speed transfer of data and commands between a main microprocessor or CPU and the SH7652 via a 16-bit bus. Use of this interface also allows network connection functions to be developed in parallel with basic user product functions, enabling development time to be shortened.

These functions enable network processing and multiple copyright protection supporting to be implemented by a single chip without imposing a load on the main microprocessor or CPU, and make possible simultaneous two channels distribution of HD digital content.

The package used is a 240-pin CSP (13 mm × 13 mm).

On-chip debugging functions are provided, and the small, PC card sized E10A-USB can be used as an emulator.

The SH7652 will be exhibited at “Embedded Technology 2006” being held at Pacifico Yokohama from November 15 to 17.

Renesas Technology will continue to extend its lineup of products with an on-chip Ethernet controller, including the provision of models offering faster CPU performance, wireless LAN support, and enhanced peripheral functions.

< Notes >

- Notes:
1. SuperH is a trademark of Renesas Technology Corp.
 2. IP broadcasting in this press release refers to the distribution of TV broadcasts via the Internet in Japan. The SH7652 comply with a Japanese broadcasting standard at the announcement.
 3. DTCP-IP (Digital Transmission Contents Protection over Internet Protocol) is a standard for IP network content protection, standardized by the DTLA (Digital Transmission Licensing Administrator). The SH7652 relating to DTCP-IP support functions were developed by Renesas Technology using technology developed by Hitachi, Ltd.
 4. WM DRM10 (Windows Multi Media DRM10) is a digital copyright technology developed by Microsoft Corporation. Microsoft, Windows, and Windows Media are registered trademarks or trademarks of Microsoft Corporation of the United States in the United States and other countries.
 5. IEEE802.3: IEEE802 is the title of an IEEE (Institute of Electrical and Electronics Engineers) committee for promoting LAN standardization. IEEE802.3 is a CSMA/CD 10/100 Mbps Ethernet LAN specification standard. In CSMA/CD (Carrier Sense Multiple Access with Collision Detection), the presence of a carrier is detected before transmission, and if a collision is detected during transmission, the system waits for a predetermined time before restarting transmission.
 6. MAC (Media Access Control): A lower sub-layer within the data link layer, stipulating the frame transmission/reception method, frame format, data error detection, etc.
 7. An SD Memory Card is a small memory card whose specification was originally formulated by 3C (Matsushita Electric Industrial Co., Ltd., Toshiba Corporation, and SanDisk Corporation) and has been progressively extended by the SDA (SD Card Association).
 8. DLNA (Digital Living Network Alliance) is an industry association that sets guidelines for the interconnection of PCs, digital home electrical products, and so forth. DLNA guidelines are guidelines for performing interconnection of products in a home network environment formulated by DLNA.
 9. MPEG-2 (Moving Picture Experts Group phase 2) is a video data compression method comprising part of the MPEG standard.

* Other product names, company names, or brands mentioned are the property of their respective owners.

< Typical Applications >

The following devices equipped with a network connection function:

- Digital audiovisual devices: DVD recorders, flat-panel TVs, audio systems, etc.
- Office automation equipment: Printers, etc.

< Prices in Japan > *For Reference

Product Name (Type Name)	Maximum Operating Frequency	Package	Sample Price [Tax Included] (Japanese Yen)
SH7652 (R5S76520B200BG)	200 MHz	240-pin CSP (13 mm x 13 mm)	2,000

< Important Note >

A license must be obtained from the DTLA (Digital Transmission Licensing Administrator) before purchase of this product.

< Specifications >

Item	SH7652 Specifications
Type name	R5S76520B200BG
Power supply voltage	1.2 V (internal) / 3.3 V (external)
Maximum operating frequency	200 MHz
Maximum processing performance	480 MIPS (at 200 MHz operation)
CPU core	SH2A-FPU (built-in double-precision floating-point unit)
On-chip RAM	32 kbytes
Cache memory	8-kbyte instruction cache memory, 8-kbyte operand cache memory (4-way set associative type)
External bus interfaces	SH local bus controller - SRAM, SDRAM, ROM directly connectable, PCMCIA interface provided - Data bus width: External 8/16/32 bits
	Host interface function - 16-bit bus width SRAM type interface - Incorporating 2 kbyte x 2 bank buffer RAM

On-chip peripheral functions	Copyright protection support functions
	- Encryption algorithms (AES/DES/3DES/MUGI): 1-block processing also possible
	- Hash algorithms (SHA-1/SHA-224/SHA-256)
	- Message authentication code generation (HMAC-SHA-1/HMAC-SHA-224/HMAC-SHA-256)
	- Dedicated DMA controller with built-in descriptor function x 2 channels
	- TTS (Time stamped Transport Stream) packet analysis
	- ProMPEG type forward error correction function
	Video stream interface x 2 channels
	- Serial/parallel switching possible
	- MPEG TS and MPEG PS both supported
	Ethernet controller x 1 channel
	TCP/IP checksum accelerator function
	Dedicated Ethernet controller DMAC x 2 channels (1 channel each for transmission and reception)
	General-purpose DMA controller x 8 channels
	Serial sound interface (SSI) x 2 channels
	- Bidirectional serial transfer
- Various serial audio formats supported	
USB 2.0 Host/Function module x 1 channel	
- High Speed/Full Speed/Low Speed supported	
- Hub function supported	
SD host interface (SDHI) x 1 channel	
- SD memory/IO card interface (1-bit/4-bit SD bus)	
I ² C bus interface x 1 channel	
Serial communication interface with FIFO (SCIF) x 3 channels (asynchronous and synchronous serial communication capability)	
16-bit compare match timer (CMT) x 2 channels	
On-chip debugging functions	
Interrupt controller (INTC)	
Watchdog timer (WDT)	
Clock pulse generator (CPG): Built-in multiplication PLL	
Power-down modes	Sleep mode
	Software standby mode
	Module standby mode
Package	240-pin CSP (13 mm x 13 mm)

Information contained in this news release is current as of the date of the press announcement, but may be subject to change without prior notice.